When Protectionism Kills Talent*

November 18, 2024

Abstract

We examine the repercussions of protectionist policies implemented in the U.S. since 2018 on workforce composition and career choices within the semiconductor industry. We find that the shift towards protectionism, aimed at reviving domestic manufacturing and employment, paradoxically resulted in a significant drop in hiring domestic talent. The effect is stronger for entry-level and junior positions, indicating a disproportionate impact on newcomers to the workforce. We also find that U.S. manufacturers, especially ones that had relied on foreign talent, reduce their domestic workforce and increase hiring overseas. Additionally, we trace the trajectories of undergraduate and graduate cohorts possessing chip-related skills over time, and document significant shifts away from the chip industry. These findings are consistent with our model, where protectionist policies aimed at revitalizing domestic employment may inadvertently lead to the opposite outcome, specifically in an industry with heavy reliance on foreign workers and inelastic labor supply.

Keywords: Chip, Economic Nationalism, Protectionism, Tariff, Workforce, Career
JEL Classifications: F16, J21, J23, O3, L1, G15

1 Introduction

The U.S. manufacturing landscape has recently seen significant shifts, notably marked by the government's turn towards protectionism in 2018 (Fajgelbaum et al., 2020). The introduction of trade tariffs aimed to increase the demand for locally manufactured products, thereby fostering domestic job creation and industry growth. As firms adjusted to tariff-induced economic pressures, their hiring and workforce management strategies were further complicated by a tightening supply of skilled labor. The "Buy American and Hire American" Executive Order in 2017, in particular, reduced the appeal of the U.S. for international students and professionals, especially engineers and scientists, seeking employment opportunities (Song and Li, 2022).[1]

In this paper, we examine the combined impact of these protectionist polices on the domestic labor markets within the U.S. manufacturing sector, with a particular focus on the semiconductor (chip) industry. We also explore shifts in global hiring strategies, asking if there has been changes in recruitment practices of U.S. firms abroad. Lastly, we assess the broader effects of these policies on the educational and career trajectories of individuals with chip manufacturing skills, observing shifts in job types and employment rates within this specialized field.

The effects of protectionist policies on labor markets are ex-ante unclear. On one hand, these policies could boost demand for local workers by encouraging companies to invest more in domestic talent and training programs. This shift towards prioritizing local workforce utilization might enhance the productivity and self-sufficiency of the domestic labor market within the semiconductor industry, though it may also present challenges in aligning skill sets with industry needs. On the other hand, increased tariffs and potential retaliatory measures from other countries could make companies more cautious in hiring, possibly reducing recruitment and making hiring more selective. Stricter immigration policies could

[1] See https://bit.ly/4aoUnD3, https://bit.ly/3TvFlVq., https://bit.ly/3PxnPij, and https://bit.ly/3voSKXb.

further constrain the supply of skilled workers, resulting in a labor shortage and hindering firms from fully benefiting from the intended stimulus of protectionist policies. These effects may ultimately lead to a decline in employment. We develop a conceptual framework to demonstrate these effects. In our model, protectionist policies aimed at revitalizing domestic manufacturing and employment may inadvertently produce opposite outcomes. Specifically, we show that these adverse effects are likely to be intensified in markets that heavily rely on foreign workers and where labor supply remains inelastic, which matches the key features of the semi-conductor industry.

To gauge the impact of protectionist policies on labor hiring and retention rates in U.S. semiconductor firms, we leverage a unique and comprehensive dataset containing detailed employee-job-employer relationships for millions of individuals employed in this sector globally. The chip industry is our focal point due to its significant susceptibility to tariff impacts, a result of its intricate global supply chains and trade dependencies.[2] Additionally, this sector has traditionally relied on an international workforce, making it particularly sensitive to shifts in immigration policies and labor market dynamics. Moreover, our dataset allows us to trace the career trajectories of individuals in this sector from their educational accomplishments to their most recent employment updates — an aspect rarely available for several other professions. Finally, the movement toward domestic chip production, though beneficial for local economies and national security, presents significant challenges, including potential talent shortages. We seek to provide detailed estimates that will inform policy discussions regarding the extent of these shortages in this strategically vital sector.

We employ a difference-in-differences methodology to examine the impact of U.S. pro-

[2]Some of the semiconductor related products affected by the tariffs include HS Codes 8541 (diodes, transistors and similar semiconductor devices); 8486.20 (machines and apparatus for the manufacture of semiconductor devices or of electronic integrates circuits), 8486.90 (machines and apparatus of a kind used for the manufacture of semiconductor boules or wafers, etc.), 8541.10 (diodes, other than photosensitive or light-emitting diodes); 8541.29 (transistors, other than photosensitive); 8541.90 (parts, diodes, transistors parts of diodes, transistors and similar semiconductor devices); 8542.31 (processors and controllers, electronic integrated circuits). Countries subject to these tariffs include China, Taiwan, South Korea, Japan, Netherlands, Germany, India, in addition to 50 other countries. Source: http://www.econ.ucla.edu/pfajgelbaum/rtp_update.pdf. See also https://bit.ly/4a5aoyc.

tectionist policies on the employment landscape for scientists and engineers within U.S. semiconductor firms, contrasting it with other job categories within the same firm-year. Our analysis reveals a notable downturn in employment indicators within these firms following the implementation of protectionist measures in 2018. Specifically, we observe a 9% reduction in hiring for scientists and engineers, contributing to a 3% decrease in their overall workforce size.[3] To provide context, the chip manufacturing sector in the United States faces an annual loss of 2,285 science and engineering positions. Between 2019 and 2022, this translates to a cumulative reduction of 9,140 jobs within the industry, which employed 66,382 engineers and 9,768 scientists during this time. While reduced hiring in chip manufacturing doesn't automatically lead to job losses for current or prospective engineers, it does signify a notable decline in employment opportunities within this sector. Moreover, there's been a similar decrease in attrition rates, resulting in a notably lower turnover of engineers and scientists post 2018.

The decline in hiring is especially acute in entry-level and junior positions, indicating that protectionist policies disproportionately affect those new to the workforce. This trend suggests recent graduates and early-career professionals in the semiconductor industry face greater challenges securing employment within the sector, potentially impacting the industry's future talent pipeline. Importantly, additional tests provide evidence that our results are not driven by recent trends in career transitions of data scientists and software engineers within the U.S. chip manufacturing industry, who are the most likely to move into similar roles in other industries. This finding rules out the possibility that our observed effects merely reflect a broader shift in tech talent towards other sectors. Instead, it reinforces that protectionist policies are having a unique and significant impact on the semiconductor industry's labor market dynamics.

We also study how the workforce of the U.S. chip manufacturers changes across their

[3]This reduction occurs despite an increase in job postings for scientists and engineers and is primarily driven by sharp declines in R&D scientist roles and specialized circuit design engineering positions, such as piping and strain engineering, which are essential for enhancing chip performance.

segments around the world (i.e., at the firm-country-job category-year level) and based on their reliance on foreign talent, particularly through the H-1B program. This setting allows us to also control for other layers of endogeneity by introducing geographic variation for each firm-year-job category. We find that U.S. manufacturers reduce their domestic workforce in the U.S. and increase hiring of more experienced workers (by 3%) outside the U.S. for both junior and mid-senior roles. The reduction in the U.S. science and engineering positions is most pronounced in firms that sponsored H-1B petitions before the ban, with the effect growing as the number of previously-sponsored petitions increases. Among the countries where U.S. chip firms have expanded their presence are Canada, which introduced favorable visa policies (Esterline, 2023), and European countries such as the Netherlands, which has an established chip manufacturing industry.[4]

Finally, we study the education and job outcomes of the cohorts of students with chip manufacturing skills. Using a difference-in-differences specification, accounting for within country-degree-job category, degree-year, country-year fixed effects, and country-degree-job category-year variation, we find that fewer number of classmates get engineering or scientist jobs alongside those with chip manufacturing skills with the start of the protectionist policies in 2018 in the U.S. The effect corresponds to a 15% drop in the number of classmates and is prevalent mostly at the undergraduate level but also at the graduate levels. The classmates of the talent in the chips industry that skip engineering and science jobs are more likely to switch to finance, marketing or other higher paying jobs. We also show that these shifts among individuals with similar educational and geographical backgrounds extend beyond the U.S. Overall, we find that there is a discernible decrease in the cohort sizes of students at both the undergraduate and graduate levels who are peers of individuals possessing chip manufacturing skills, indicating a waning interest in chip manufacturing industry, especially in the U.S.

[4]We also test for the parallel trends by showing that the time-specific treatment effects show no pre-trends in any of our tests. We in fact see strikingly parallel trends for treatment and control job categories before 2018 and a clear change in only the treated group afterwards.

Our paper is mainly related to the vast literature that studies the effects of trade frictions on labor markets. Along these lines, Irwin (2000) discusses the effect of tariffs on growth in 19th century America. In the context of how the 2018 trade war affected companies and local economy in particular, Fajgelbaum et al. (2020) demonstrate substantial declines in both imports and exports following the imposition of increased tariffs in the U.S. and retaliation by trade partners (Goldberg and Pavcnik, 2016; Flaaen and Pierce, 2019). This led to significant losses exceeding $50 billion for U.S. consumers and firms purchasing imported goods, resulting in an aggregate real income reduction of $7.2 billion (0.04% of GDP) when considering tariff revenues and gains to domestic producers. Amiti, Redding and Weinstein (2019) similarly estimates significant losses attributable to the 2018 import tariffs for U.S. consumers and firms, amounting to approximately $3.2 billion per month in additional tax costs and an additional $1.4 billion per month in deadweight welfare losses. Utilizing Burning Glass Technologies data, Javorcik, Stapleton, Kett and O'Kane (2022) show a 0.6% decrease in online job postings in commuting zones affected by input tariffs and retaliations by trading partners in 2018. These effects were more pronounced for lower-skilled job postings compared to higher-skilled ones.

We also contribute to the literature on the *China shock.* Autor, Dorn, Hanson and Song (2014) document the adverse effects of heightened imports from China between 1992 and 2007 on employment, labor force participation, and wages within manufacturing industries competing with more affordable imports. Additionally, they illustrate the substantial adjustment costs for individual workers resulting from this import shock, with higher-wage workers experiencing relatively better outcomes compared to their lower-wage counterparts. Pierce and Schott (2016) study the effect of the elimination of potential tariff increases on Chinese imports in 2000 on employment, and Autor, Dorn and Hanson (2013), Acemoglu et al. (2016), Caliendo et al. (2019), and Autor, Dorn and Hanson (2021) analyze the impact of the *China shock* on wide range of outcomes, including the labor market, between 2000 and 2019. Stanig and Colantone (2018) argue that this trade shock from China has led to

political polarization and increased nationalism around the world. Cen et al. (2023) study how U.S. firms used their internal capital markets to stay resilient to the five year plans of China between 2001 and 2016, which lead to significant drops in both employment and investments in the same sectors in the U.S. They show that firms adjusted by shifting production to upstream or downstream industries, offshoring to supported industries in China. Hombert and Matray (2018) find that Chinese imports slow growth and reduce profitability, but firms with more R&D are less affected due to increased product differentiation, resulting in smaller cuts in capital and employment.[5]

Our paper is also related to the literature on the effect of political uncertainty on firm investment and employment. Baker et al. (2016) develop a measure of economic policy uncertainty and show that it is associated with reduced firm-level investment and employment. Bloom et al. (2022) argue that economic uncertainty in the world has been rising significantly with various major uncertainty shocks, including China-U.S. trade-tensions, within the last decade. Their research shows that these shocks have real consequences for companies. See also Campello and Kankanhalli (2022) for a review of the literature on corporate decision making under uncertainty.[6] There is also a growing literature on the effects of work (H1-B) visas on firm and worker outcomes (see, e.g., Doran, Gelber, and Isen (2022)).

Lastly, our paper adds to the literature on economic nationalism. Dinc and Erel (2013) provide evidence of prevalent economic nationalism in government responses to significant corporate merger attempts in Europe, where local authorities exhibit a preference for target companies to remain under domestic ownership rather than foreign control. Morse and Shive (2011) analyzes the impact of patriotism on equity investments, while Gupta and Yu (2007) explore bilateral capital flows. D'Acunto, Huang, Weber, Xie and Yang (2023) shows hiring restrictions on high-skilled foreign nationals, exemplified by the 2007 Employ American Workers Act led to reduced patent filings in FinTech, cybersecurity, and payment

[5]Also see Bernard et al. (2012, 2006); Frésard and Valta (2016); Xu (2012); Valta (2012) on the effects of imports on leverage, cost of debt, capital investments, and outsourcing. See Hoberg and Phillips (2016) on product differentiation.

[6]See, e.g., Alfaro et al. (2024) for the effects of financial uncertainty on firm employment

systems, alongside increased wage premiums paid to retain pre-crisis foreign hires.

2 Why Semiconductor Industry?

The broad impact of protectionist policies plausibly affected many of the U.S. manufacturing sectors. We focus on the semiconductor sector, because of three reasons.[7] First, the semiconductor industry relies heavily on international talent (Ozimek and O'Brien, 2023) and collaboration for innovation and competitiveness (Jones and Lotze, 2023; Bown and Wang, 2024). Protectionist measures, such as tariffs and immigration restrictions, disrupt the flow of skilled professionals and hinder international collaboration, thereby impeding the industry's ability to innovate and adapt to changing technological landscapes. Second, the semiconductor industry operates in a highly interconnected global supply chain (Thadani and Allen, 2023). Tariffs on imported raw materials and components increase production costs for semiconductor manufacturers, making it more challenging for them to remain competitive in the global market. Additionally, retaliatory tariffs from trading partners decrease demand for American semiconductor products abroad, further impacting the industry's profitability and growth prospects. Third, our aim is tracing individuals' career trajectories and identifying their skill sets. Analyzing how individuals adapt their careers to protectionist shocks necessitates examining millions of resumes. Our data is especially apt for studying the semiconductor industry, as many individuals in this industry voluntarily disclose their information, which is not commonly observed in other manufacturing sectors (top three industries that constitute the greatest number of resumes on this platform are financial services, information technology and services, hospital & health care).

Historically, the United States (Texas Instruments, Fairchild Manufacturing, and Intel) led chip manufacturing until the 1980s. Japan (Toshiba, NEC, and Hitachi), followed by

[7]There are not many papers studying the dynamics of workforce in specific industries. The closest study to ours is Angel (1989) which investigates the labor market organization and geographic concentration of engineers in the U.S. semiconductor sector. Angel's use of survey data shows a pronounced localization of this workforce in Silicon Valley, underscoring the region's pivotal role in the industry.

South Korea (Samsung), China, Taiwan (notably TSMC), and select European countries (such as ASML Holding from the Netherlands), have markedly expanded their market share in recent years. Presently, the U.S. accounts for a mere 10 percent of global commercial chip production, yet it maintains its leadership in design, research, and development.[8] Chip production entails processing such as design, manufacturing, and packaging. Integrated Device Manufacturer (IDM) companies like Intel encompass all these facets, while Fabless entities like Qualcomm focus solely on design, and Foundry firms such as TSMC specialize in manufacturing semiconductors designed by Fabless companies. The semiconductor industry comprises both memory and logic chips markets, with the latter dominating (approximately 70 percent). While South Korea leads in memory chips, necessitating economies of scale for mass production, the U.S. concentrates on logic chips, demanding skilled architects leveraging cutting-edge technology. Geographically, chip manufacturing remains highly concentrated, posing significant supply chain risks (NIST).

The globalization wave in chip manufacturing, catalyzed by events like China's entry into the World Trade Organization (WTO), has encountered headwinds. Trends towards nationalist economic policies post-global financial crisis and exacerbated by the COVID-19 pandemic have spurred a shift towards homeland economics. Recognizing the strategic importance of chip manufacturing, particularly in bolstering national security, initiatives like the 2021 Facilitating American-Built Semiconductors (FABS) Act and the 2022 CHIPS and Science Act have emerged. These measures encompass substantial investment tax credits and grants to stimulate domestic chip manufacturing and research while prioritizing investment in American workers (see the White House briefing, August 9, 2022).

3 Conceptual Framework

To motivate and provide a framework for interpreting our empirical findings, we introduce a model in which consumers demand chips and other goods, and chip firms decide on hiring

[8] See http://www.chips.gov.

levels and production quantities amid protectionist policies. We demonstrate that protectionist policies can lead to reduced hiring and production among U.S. chip firms. Notably, the hiring decline is most pronounced when the sector relies heavily on foreign workers and labor supplies are inelastic.

Demand for chip products

There is one representative consumer that demands both chips and other products, which we denote by, Y_C and Y_O, respectively. We assume that the consumer has a standard CES (constant elasticity of substitution) utility, like in Fajgelbaum et al. (2020). The consumer chooses the consumption bundle to maximize its utility:

$$u = \max_{Y_C, Y_O} \left(\alpha_C^{\frac{1}{\eta}} Y_C^{\frac{\eta-1}{\eta}} + \alpha_O^{\frac{1}{\eta}} Y_O^{\frac{\eta-1}{\eta}} \right)^{\frac{\eta}{\eta-1}}, \tag{1}$$

subject to the budget constraint:

$$Y_C \times P_C + Y_O \times P_O = I, \tag{2}$$

where α_C and α_O are the share parameters corresponding to chips and the bundle of other products in the consumer's utility function. I is the household's budget constraint.

We model the supply of other products as perfectly elastic at a price of P_O, treated as exogenous, primarily to simplify our equilibrium calculations. The main intuitions remain the same if the supply is elastic. Chip products are supplied by J symmetric U.S. firms, whose production decisions are detailed below.

Production environment

A chip manufacturer uses domestic and foreign labor as inputs to produce chip products under a Cobb-Douglas production function:

$$y = z\left(d + f\right)^{\theta}, \tag{3}$$

z represents the firm's total factor productivity (TFP), and d and f denote domestic and foreign labor hired, respectively. We do not explicitly include capital in the production function, assuming instead that firms rent productive capital from a competitive intermediate goods market, with these decisions optimized out.

The firm chooses its employment to maximize profit, net of wage costs.

$$\pi_j = \max_{\{d_j, f_j\}} (P_D - v) z\left(d + f\right)^{\theta} - W^D \cdot d - W^F \cdot f, \tag{4}$$

where P_C represents the market price for chip products, and v denotes the variable cost per unit of output, covering costs such as raw materials, shipping, delivery, and utilities. The wage rates for domestic and foreign workers are $\{W^D, W^F\}$, which will be determined in equilibrium.

Taking the first-order condition of the firm's profit with respect to domestic and foreign employment yields the firm's optimal labor demand:

$$z(P_D - v)\theta\left(d + f\right)^{\theta-1} = W_D \tag{5}$$

$$z(P_D - v)\theta\left(d + f\right)^{\theta-1} = W_F \tag{6}$$

The equations above suggest that, in equilibrium, the wage rate for domestic and foreign workers will satisfy $W_D = W_F \equiv W$, which also equals the marginal revenue product of labor.

The repercussion of protectionist policies

We model the repercussions of protectionist policies as having three main effects: first, they provide investment subsidies, particularly on R&D investments and various talent development programs. Such investments increase the firm's TFP, raising the marginal product of labor. Second, they restrict the hiring of foreign labor. Specifically, we assume that at any given wage level, only a fraction, $\lambda(< 1)$, of foreign workers willing to work for U.S. chip manufacturers can obtain a work visa. We denote the labor supply curves of domestic and foreign workers by $S_D(\cdot)$ and $S_F(\cdot)$, respectively. Protectionist policies shift the foreign labor supply curve to $\lambda S_F(\cdot)$, while the domestic labor supply curve remains unchanged. Lastly, protectionist policies impose tariffs on raw materials and intermediate inputs sourced from foreign countries, which can increase domestic firms' production cost, v, and reduce their profit margins.

Equilibrium price and wage

Proposition 1. *There is a unique combination of equilibrium wage rate, W, and price for chip products, P_C, which are characterized by:*

$$J \times \left[\frac{W}{z\theta(P_C - v)}\right]^{\frac{1}{\theta-1}} = S_D(W) + \lambda S_F(W), \tag{7}$$

and

$$J \times z\left[\frac{W}{z\theta(P_C - v)}\right]^{\frac{\theta}{\theta-1}} = \alpha_C I P^{\eta-1} P_C^{-\eta}, \text{ where } P^{1-\eta} = \alpha_C P_C^{1-\eta} + \alpha_O P_O^{1-\eta} \tag{8}$$

Equation (7) is derived from the labor market clearing condition, which states that the aggregate labor demanded by all J firms (LHS of Equation 7) must equal the total number of domestic and foreign workers willing and able to supply labor at the equilibrium wage rate (RHS of Equation 7).

Equation (8) is based on the product market clearing condition, which states that the total production by domestic firms (LHS of Equation 8) must equal the representative consumer's

demand (RHS of Equation 8). This demand is negatively related to the price of chips and positively related to the overall price index P, which is a weighted average of the price of chips and that of other products. Since we assume the latter is supplied elastically at a price of P_O, we are left with two equations and two unknowns. We show that this system of equations yields a unique combination of equilibrium price and wage rate.

By using Equation (8), we can express the equilibrium wage rate as a function of the product prices and substitute it into Equation (7). Applying the implicit function theorem, we can then analyze the relationship between equilibrium employment and the intensity of protectionist policies.

Proposition 2. *Investment subsidies would increase equilibrium employment, whereas more stringent H-1B restrictions or higher tariffs on raw materials would lead to a monotonic decrease in equilibrium employment.*

Higher investment subsidies prompt firms to adopt more advanced technology, increasing the marginal revenue product and stimulating labor demand. However, if protectionist policies also raise the price of raw materials, this would partially offset the increased marginal product of labor, creating an opposite effect. We refer to these two effects as the "firm demand channel," as they primarily influence the profitability of production for firms.

When H-1B restrictions become more stringent, they reduce labor supply by shifting the labor supply curve inward. Consequently, firms must move up the supply curve to attract additional workers, resulting in higher wage payments, higher production costs, and lower quantity demanded in the equilibrium. We refer to this as the "labor supply channel." From the above discussion, we can see that the overall effect of protectionist policies is unclear, as it depends on the relative magnitudes of these channels.

Proposition 3. *The stimulative effect of investment subsidies diminishes when labor supplies are more inelastic and H-1B restrictions are more stringent.*

While Proposition 2 examines the individual effects of the subsidies, tariffs, and labor

market protection policies, this proposition focuses on the interaction between the firm demand and labor supply effects. It suggests that the stimulative impact of investment subsidies on equilibrium hiring may be limited when H-1B restrictions are stricter and labor supplies in the chip industry are more inelastic.

Introducing an investment subsidy incentivizes firms to enhance their technology and production efficiency, which, in turn, lowers the per-unit price of chip products. As households increase their demand for chips, firms need to scale up production, requiring them to hire more workers. This heightened demand for labor pushes up the wage rate for chip workers, thereby increasing production costs for chip firms. When labor supply is less elastic—likely due to the specialized training and challenging work conditions in the chip industry, which limit the pool of eligible and willing workers—the rise in wages becomes more pronounced, driving up chip product prices even further. This price increase partially offsets the initial price decline resulting from more efficient production technology. In such conditions, the stimulative effects of investment subsidies on production and employment are likely to be dampened.

Proposition 4. *The negative effect of H-1B restrictions becomes more pronounced when foreign workers constitute a larger share of the labor market and when labor supplies are less elastic.*

Proposition 4 states that a less elastic labor supply not only dampens the stimulative effect of investment subsidies but also intensifies the adverse effects of H-1B restrictions, further decreasing equilibrium hiring. Essentially, when foreign workers comprise a larger portion of the labor market, H-1B restrictions impact a broader group, causing a more significant reduction in employment. With a less elastic labor supply, firms must raise wages substantially to compensate for the labor shortfall created by these restrictions. This wage increase raises production costs and chip prices, leading to decreased demand, reduced production, and, ultimately, lower equilibrium employment.

We can also view the results of Propositions 3 and 4 from a cross-sectional perspective.

According to our model, when comparing workers across different occupations within the same chip firm under the same set of product and labor market protectionist policy, occupations with a higher proportion of foreign workers and less elastic labor supplies will experience a greater decline in equilibrium hiring than occupations primarily composed of domestic workers with relatively more elastic labor supplies.

Model Discussion

In the discussion above, we primarily focus on how protectionist policies affect the first moment of various model primitives. However, in practice, these policies can also impact the second moment. For instance, chip firms may face uncertainty regarding the timing and specific form of investment subsidies. Additionally, higher tariffs could provoke retaliatory actions from other countries, affecting firms' export opportunities. Under such uncertainty, and assuming firms are risk-neutral, our model indicates that firms will continue to follow the same labor demand decisions as characterized by (5) and (6). However, workers, being risk-averse, will base their labor supply decisions on the certainty equivalent of wage income. The total labor supply by domestic and foreign workers thus can be represented by $S_D(W - \rho_D\sigma^2) + \lambda S_F(W - \rho_F\sigma^2)$. As protectionist policies increase uncertainty, labor supply will further decrease through this uncertainty channel. All of our propositions remain valid when accounting for this uncertainty channel.

4 Data

We use Revelio Labs database to obtain detailed information on employee, employer and job characteristics.[9] Revelio Labs positions itself as a company that collects and standardizes hundreds of millions of publicly available employment records to create "world's first universal HR database" enabling users to track the workforce dynamics and trends of any organization. The data includes nearly a billion employees around the world across all in-

[9]See, for example, Amanzadeh et al. (2024) using the same data vendor.

dustries, scraped as of March 2023. In this data, we narrow our focus on the workforce with chip-related skills or workforce that have ever worked in the chip industry as well as their classmates from college or graduate schools (irrespective of the industries of their jobs).

The data allows us to observe each employee's current as well as past jobs, skills, location, educational background, job category, seniority, various personal characteristics like estimated age and gender, as well as employer characteristics. Using this data, we first provide various statistics on the workforce in the global chip manufacturing industry before moving on to testing the specific hypothesis laid out above. Section 4.1 provides key summary statistics on active semiconductor workforce around the globe, in addition to employment characteristics within the U.S. chip manufacturing industry (Section 4.2), and job market outcomes for cohorts of potential chip manufacturing talent after graduation (Section 4.1.3). We provide a detailed summary of our data collection process in Appendix Section B.1.

4.1 Active Semiconductor Workforce

Table 1 provides the distribution of the physical location of 1.6 million active employees with chip manufacturing skills as of March 2023 across the world. Note that these people are not necessarily working for a chips company, nor are they necessarily working for a local company, all of which we will address later. United States is at the top of the list of countries hosting these skills, with 680,602 employees being physically in the US.[10] A large fraction (480,193) of these employees work as an engineer, while 49,515 are scientists. An average employee has been at her current job, which is the 5.5^{th} one over her career, for 2,819 days (almost 8 years), with an average seniority of level 3 (associate level) out of 7.

[Table 1 about here]

[10]To assess Revelio's coverage, we compared its data with the Statistics of U.S. Businesses (SUSB) Annual Data Tables, focusing on five 6-digit NAICS codes relevant to our study: 333242, 333994, 334413, 334418, and 334515. In 2017, Revelio reported 2,070 firms in these categories, while the U.S. Census documented 2,653. This comparison indicates that Revelio's dataset captures a substantial portion of the U.S. chip manufacturing industry, providing a reliable representation of the sector.

India has 165,352 employees with chip skills and a larger fraction of these people (almost 130,000) are engineers. The United Kingdom ranks third with a total of 88,527 employees, heavily skewed towards engineering roles with 57,927 engineers. Table 1 further illustrates that countries such as India, Brazil, Pakistan, Turkey, and Malaysia have a significant number of engineers with chip manufacturing skills and experience, as indicated by their job positions and tenure lengths. We discuss the detailed characteristics of these countries and the rest of the world in Section B.1.2 of the Appendix to save space. Figure 1 further illustrates the global distribution of employees with chip manufacturing skills who are actively employed as of March 2023, including countries not shown in Table 1.

[Figure 1 about here]

4.1.1 Chip Manufacturing Skills in the U.S.

While Table 1 shows the United States as the leading country in terms of the number of employees skilled in chip manufacturing, it does not specify the particular skills these employees possess. Therefore, Figure 2 highlights the list of skills utilized to identify individuals with chip manufacturing expertise, alongside the percentage representation of each skill among employees in the U.S. The variation in skill distribution reveals both the core and peripheral abilities that contribute to the U.S. chip manufacturing sector's operational breadth.

[Figure 2 about here]

As shown in Figure 2, skills such as *Plasma Etch* (71.99%), which is a critical skill in the fabrication of semiconductors for carving fine patterns on the surface of silicon wafers, and *Design Of Experiments* (67.67%), another important skill for estimating defect and scrap rates, which is critical to maximize profitability, exhibit substantial prevalence in the American workforce. Similarly, *Chemical Vapor Deposition* (67.39%), used to create high-quality thin films, underscores its importance. Beyond these specialized skills, our dataset

encompasses broader skill categories, including *Semiconductor Manufacturing*, where 57.58% of the global workforce is based in the US.

On the other end of the spectrum, other skills such as *Proteus* (9.98%), an important skill for reducing carbon footprint of semiconductor manufacturing, *Autosar* (11.32%), a critical skill in the design and development of automotive electronics, which are increasingly dependent on sophisticated semiconductor devices, and *Electrical Machines* (15.18%), which refers to knowledge in operating electrical machinery, reveal a lesser extent of representation.[11] Overall, Figure 2 indicates that the US holds a leading role in certain key skills within the chip manufacturing sector, yet there remains room for expanding its presence in additional skill areas.[12]

The above findings indicate that while the U.S. has the highest number of employees with chip manufacturing skills, it does not dominate in every specific skill within the chip manufacturing sector. A considerable portion of these skills are found in the workforce outside the U.S. This leads to questions regarding the utilization of individuals possessing chip manufacturing skills. To address this, our subsequent analysis focuses on the employment distribution of chip manufacturing talent. We begin by identifying the companies that employ these individuals and then assess their distribution across various industries, comparing those directly involved in chip manufacturing with those in unrelated sectors.

[Table 2 about here]

4.1.2 Top Employers of Top Chip Manufacturing Skills

Table 2 provides the list of top employers of the global workforce with chip manufacturing skills. Intel Corporation is not surprisingly the number one and the U.S. government, perhaps more surprisingly, is the number two in the list, with almost 30,000 and 13,400 em-

[11] In February 2024, the Biden-Harris Administration announced a deal to allocate $1.5 billion from the CHIPS and Science Act to enhance semiconductor production related to the U.S. auto industry. See https://bit.ly/3I3e3R1.

[12] See, e.g., more information on Plasma Etch, Design of Experiments, Chemical Vapor Deposition, and Autosar.

ployees respectively.[13] Government entities such as the United States Navy, US Air Force, The United States Army, Sandia National Laboratories, Jet Propulsion Laboratory, Federal Aviation Administration, US Department of Defense, Lawrence Livermore National Laboratory, and the National Aeronautics & Space Administration are notable employers of individuals skilled in chip manufacturing. Qualcomm is in the top five of employers, with similar number of employees (10,000–11,000) to Apple and Amazon, which seem to have hired individuals with these skills. This said, based on the seniority composition in Table 2, Apple and Amazon hired employees with chip skills before the protectionist era and/or primarily for senior, rather than junior, roles.

There are also non-US companies like Siemens from Germany and NPX Semiconductors from Netherlands in this top list. The "Other Employers" category encompasses a significant portion of the workforce, highlighting the extensive demand and versatility of chip manufacturing skills across diverse sets of companies and sectors. Overall, the table illustrates a wide-ranging employment spectrum for professionals with chip manufacturing capabilities, extending from conventional chip manufacturing firms to governmental agencies and software companies worldwide.

Table 2 also showcases the concentration of expertise and experience within these organizations. Intel Corp stands out with the majority of its 15,397 employees at Seniority Level 2, emphasizing a strong mid-level expertise in its workforce. Qualcomm Inc, with 3,461 employees, sees its largest group at Seniority Level 4, suggesting a workforce with advanced experience and expertise. At the more advanced Seniority Levels 5, 6 and 7, Intel Corp leads, highlighting its leadership in highly experienced and specialized personnel.

[Table 3 about here]

Table 3 delves into the industry composition of 680,602 active workforce with chip manufacturing in the U.S. Panel A identifies core chip manufacturing sectors, with "Semiconductor

[13] We conducted additional analyses to validate our employee count data, focusing on key chip manufacturers central to our study (not tabulated). For example, our records show Intel with over 119,000 employees in 2022, aligning closely with publicly reported figures of approximately 120,000 employees.

and Related Device Manufacturing" leading at 72,512 employees, followed by "Semiconductor Machinery Manufacturing" and "Instrument Manufacturing for Electricity & Electrical Signal Testing" with 7,943 and 6,514 employees, respectively. Panel B explores employment in non-chip manufacturing industries, where "Software Publishers" top the list with 35,572 professionals, and "Colleges, Universities, and Professional Schools" employ 27,661. These include academic positions, post-docs, researcher roles at universities and related labs. Other significant sectors include "Radio/TV Broadcasting & Wireless Communications Equipment Manufacturing" and "Internet Publishing and Broadcasting and Web Search Portals," housing 14,591 and 13,512 professionals, respectively.

To summarize, this section shows that the U.S. is at the forefront in terms of active chip manufacturing workforce, housing approximately 600,000 of the global 1.6 million experts in this field. However, it appears that the U.S. does not fully capitalize on its chip manufacturing workforce's potential, because many individuals with chip manufacturing skills work at jobs outside the chip manufacturing industry.

4.1.3 Yearly Cohorts of Students Proficient in Chip Manufacturing Skills

Using our unique data covering education characteristics of various cohorts of students around the world, we also present summary statistics on chip manufacturing education and job outcomes. Figure 3 offers a look into the first career steps taken by U.S. graduates who shared the same graduation year, program, and university with individuals possessing chip manufacturing skills. This analysis is segmented by degree type and initial job category chosen post-graduation. For job category classification, we employ Revelio's clustering algorithms, which sort jobs into seven primary categories: Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist. The data is as of the end of 2017, and the figure excludes counts of classmates below 1,000 to enhance readability.

[Figure 3 about here]

The cohort size for the year 2017 totals 109,126. Bachelor's degree holders (65,290) predominantly pursued engineering, with 42,100 graduates, followed by roles in science (6,184) and sales (5,862). For those with Doctoral degrees, a pronounced preference for scientific (2,180) and engineering (1,282) positions emerges, underscoring a career focus on research and technical development within the chip manufacturing field. Master's degree recipients show a preference for engineering (25,693) and science (3,600), with additional graduates moving into administrative, financial, marketing, operational, and sales positions. MBA graduates display a diverse range of initial job preferences, with significant numbers entering engineering (1,136) and sales (1,043), alongside finance (801) and operations (543).

Overall, Figure 3 illustrates that prior to the U.S. protectionist policies, individuals with a Bachelor's degree exhibited a preference for roles within technical and commercial sectors. Those with Doctorate and Master's degrees predominantly pursued careers in science and engineering. On the other hand, there is a tendency among MBA graduates to seek positions that combine technical expertise with strategic and commercial insight.

4.2 U.S. Chip Manufacturer Firms

In this section, we provide descriptive statistics for U.S. manufacturing firms over the period from 2014 to 2022. It is important to note that, unlike in the previous section, we do not focus on workforce with chip manufacturing skills nor their education cohorts, but, instead, on every employee that work at chip manufacturers independent of their skills reported. The dataset is organized at firm, job category, and year. For job category classification, again, we employ Revelio's clustering algorithms, which sort jobs into seven primary categories: Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist. In particular, the categories include a broader range of roles beyond engineers and scientists, reflecting the diverse workforce within U.S. chip manufacturer firms around the globe.

[Figure 4 about here]

Figure 4 displays the aggregate number of employees categorized by job descriptions as

of the end of 2017. As shown, the total employment across all job categories in the chip manufacturing industry stands at 170,636.[14] This suggests an average of 148 employees per firm, or alternatively, 21 employees for each firm-job position tuple. The largest single group is Engineers, holding 66,382 positions. Administrative roles make up 16,822 of these positions, while Operations and Sales roles account for 20,072 and 30,890 positions, respectively. Furthermore, Marketing and Finance roles contribute 12,710 and 13,992 positions, respectively. Additionally, there are 9,768 Scientist roles, emphasizing the industry's investment in research and development.

[Table 4 about here]

Panel A of Table 4 provides further summary statistics for various employment metrics across 68,949 firm-job category-year observations over 2014-2022 time period. We focus on the logged values of employee counts, hiring, separation, and turnover rates, alongside specific hiring categories. The average of $\text{Log}(\text{Emp}_{i,j,t})$ stands at 1.76, with a median of 1.39. The means for $\text{Log}(\text{Hiring}_{i,j,t})$ and $\text{Log}(\text{Separation}_{i,j,t})$ are 0.62 and 0.59, respectively, while $\text{Log}(\text{Turnover}_{i,j,t})$ has a higher average at 0.88. In terms of specific rates, the Hiring $\text{Rate}_{i,j,t}$ averages at 0.16, whereas the Separation $\text{Rate}_{i,j,t}$ is slightly lower at 0.12, suggesting a trend of more hiring than separation.[15] The Net Hiring $\text{Rate}_{i,j,t}$ averages at 0.04, indicating the balance between hiring and separation. The Turnover $\text{Rate}_{i,j,t}$ is higher at 0.28.

The breakdown into specific hiring categories shows that experienced (first-time) employees have the mean log value at 1.56 (0.95), suggesting that firms are more inclined towards hiring experienced individuals. Employees with junior and mid-senior positions, ($\text{Log}(\text{JunPosEmp}_{i,j,t})$ and $\text{Log}(\text{MidSenPosEmp}_{i,j,t})$), exhibit lower averages, indicating a lesser but significant volume of hiring in these categories.[16] These statistics collectively

[14] U.S. Census Bureau reports 207,377 chip manufacturing employees in 2017. Source: Annual Data Tables from the Statistics of U.S. Businesses (SUSB) with 6-digit NAICS codes of 333242, 333994, 334413, 334418, and 334515.

[15] The mean values of $\text{Emp}_{i,j,t}$, $\text{Hiring}_{i,j,t}$, and $\text{Separation}_{i,j,t}$ are 70.33, 9.41, 7.31, respectively.

[16] The mean values of $\text{FirstJobEmp}_{i,j,t}$, $\text{ExprEmp}_{i,j,t}$, $\text{JunPosEmp}_{i,j,t}$, $\text{MidSenPosEmp}_{i,j,t}$ are 15.55, 54.78, 47.52, 21.02, respectively.

provide insights into the hiring patterns and workforce dynamics within firms, highlighting the prevalence of experienced hires and the general trends in employee turnover. Panel B displays similar statistics for the U.S. firms across its domestic and international segments.

5 Empirical Strategy and Main Findings: Talent in U.S. Chip Manufacturing Companies

In this section, we discuss our empirical methodologies and main findings. We will start with our approach to estimating the impact of U.S. protectionism on worldwide employment in science and engineering roles within U.S. chip manufacturing companies.[17]

We estimate the average treatment effect of post-2018 U.S. protectionism on science and engineering jobs at U.S. semiconductor manufacturing firms by running the following difference-in-differences regression:

$$y_{i,j,t} = \beta \text{Treated}_j \times \text{Post}_t + \alpha_{i,t} + \delta_{i,j} + \epsilon_{i,j,t}, \tag{9}$$

where i denotes the firm, j denotes the job category, and t represents the year. Our study focuses on several key dependent variables $y_{i,j,t}$, which include the logarithm of the number of employees ($\log(\text{Emp}_{i,j,t})$), hiring ($\log(\text{Hiring}_{i,j,t})$), separation ($\log(\text{Separation}_{i,j,t})$), and turnover ($\log(\text{Turnover}_{i,j,t})$). We also examine rates such as the hiring rate ($\text{Hiring Rate}_{i,j,t}$), separation rate ($\text{Separation Rate}_{i,j,t}$), net hiring rate ($\text{Net Hiring Rate}_{i,j,t}$), and turnover rate ($\text{Turnurnover Rate}_{i,j,t}$) across different job categories and time periods.

The variable $Treated_j$ is assigned a value of one for science and engineering job categories, and it's equal to zero for finance, marketing, sales, operations, and administrative job categories. $Post_t$ takes a value of one for the years post-2018 and zero for the preceding years, and $\epsilon_{i,j,t}$ is the disturbance term. The coefficient of interest in Equation (9) is β,

[17]Note that, in this section, our sample contain employees of U.S. semiconductor companies around the world, rather than people with chip skills who might be working in any company.

associated with $Treated_j \times Post_t$. It quantifies the homogeneous average treatment effect of U.S. protectionism on science and engineering jobs at U.S. chip manufacturing firms.

The main challenge in estimating the directional effect of U.S. protectionism is discerning how firms' anticipatory actions, like strategic hiring, stockpiling, lobbying, or supply chain diversification, might skew our understanding of protectionism's effect on science and engineering employment. We therefore incorporate firm-job category fixed effects $\delta_{i,j}$ and firm-year fixed effects $\alpha_{i,t}$. The former adjusts for fixed characteristics of firms' departments, recognizing that, for instance, some might naturally have large engineering/research or sales teams.

Firm-year fixed effects allow for an intra-firm comparison of employment across various job categories, using non-engineering and non-scientist roles within the same year as counterfactual. For example, they allow us to compare the number of people working in Qualcomm's science and engineering teams with the number of people in Qualcomm's sales, marketing, operations, and admin teams in the same year. In doing so, our key identifying assumption is parallel trends, which we will discuss later.

Sample period covers years between 2014 and 2022, leaving four years before and after the 2018 shock. All specifications include firm-job category as well as firm-year fixed effects. Standard errors are corrected for clustering of observations at the firm level.[18]

5.1 Main Findings

We present our main findings on the impact of U.S. protectionism on the employment of scientists and engineers, in comparison to other job categories, within the U.S. semiconductor firms –i.e., findings from the main difference-in-differences specification as detailed in Equation (9)– in Table 5.

[Table 5 about here]

[18]This method accounts for unobserved correlations within a firm, possibly causing correlated disturbances in our analyses. Such correlations might arise from changes in firm policies, fundamentals, or other factors influencing multiple job categories within the same firm simultaneously.

As shown, the coefficient on the treated-post interaction is negative and significant at the 1% level in all specifications in Panel A, with -0.03 for the log employment (Column 1), -0.09 for log hiring (Column 2), -0.04 for log separation (Column 3), and -0.09 for log turnover (Column 4). In other words, firms in the chip manufacturing industries experienced a significant decline in employment and hiring counts. They also experienced a similar decline in attrition, leading to a significantly smaller turnover of engineers and scientists starting in 2018.[19]

Based on our findings shown in column (1) of Table 5 along with descriptive statistics from Figure 4, the U.S. experiences a yearly loss of 2,285 science and engineering jobs ($3\% \times (66,382 + 9,768)$) in the chip manufacturing sector. From 2019 to 2022, during the post-treatment period, this amounts to a total reduction of 9,138 jobs in this industry. According to Figure 3, 67,793 engineers ($42,100 + 25,693$) and 9,784 scientists ($6,184 + 3,600$) graduate with undergraduate and master's degrees each year, positioning them as ideal candidates for these roles. While the decrease in job opportunities in the chip manufacturing industry doesn't necessarily imply these students will be unemployed, it does indicate a considerable reduction in their employment prospects within the chip manufacturing field.

[Figure 5 about here]

Figure 5 provides clear evidence supporting the observable counterpart of the parallel trends assumption, which is essential for the difference-in-differences method we used in Table 5. It shows the time-specific treatment effects of protectionism on the number of science and engineering jobs at U.S. chip manufacturers, revealing no discernible pre-trends in either variable. Post-treatment, the number of science and engineering jobs experiences a rapid and sustained decline. The second panel of the figure separates the fitted trends into treated and control groups.[20] This panel is crucial to counter the argument that the

[19] In Appendix Table B6, we confirm that our results hold after using Poisson regression analysis.

[20] Using fitted trends is advantageous because it ensures treated and control groups start from the same point, making it easier to check if their trends were parallel before the treatment. This method clearly shows where these trends begin and end. For more details on fitted trends, see `estat trendplots`: https:

estimated effects on science and engineering jobs might be due to a rise in non-technical roles, such as marketing or legal positions, within the control group. This said, given the broad impact of protectionism, it's also reasonable to anticipate a general decline in job numbers, suggesting our estimates could be conservative. This panel helps us understand which argument is backed by the data.

The second part of Figure 5 shows strikingly parallel trends for treatment and control job categories before the beginning of U.S. protectionism. However, for the treated group, there is a clear drop in job numbers after the beginning of U.S. protectionism. Conversely, the control units continue to exhibit trends consistent with the period before the beginning of U.S. protectionism, showing little to no change in their persistence. For brevity, we only present effect dynamics of column (1) here. Figures B3 and B4 of the Appendix document effect dynamics associated with other variables.

Overall, these findings align with our model's predictions, demonstrating that protectionist policies can negatively impact the labor dynamics of U.S. chip firms. Specifically, we observe an unsustained growth rate of employment in non-science and engineering occupations and a sharp decline in science and engineering employment. This occurs when the reduction in labor supply due to protectionist measures outweighs the policies' stimulative effect on firm demand. Moreover, the comparison across occupations reveals that protectionist policies disproportionately affect scientists and engineers. This is consistent with our model's prediction that the overall adverse effects of such policies are particularly pronounced in occupations heavily reliant on foreign workers and characterized by relatively inelastic labor supply.

Next we study the hiring and attrition rates, using a similar estimation method as in the previous table. As shown in Panel B of Table 5, we see a significant post-2018 drop not only in the hiring rate but also the attrition rate for engineers and scientists, in comparison to

`//www.stata.com/manuals/tedidregresspostestimation.pdf`. Due to convergence issues with Stata's `xtdidregress` command, we limit our trend analysis to fixed effects for both firm-job category and year. Figure B1 in the Appendix plots observed means using the same command.

other job categories within the same firm-years. The coefficients are -0.03 and -0.02, both statistically significant at the 1% level. When we use net hiring rate, which is defined as the difference between the two, we still see a statistically and economically significant coefficient of -0.02. In the last column, we present results for the turnover rate, which is the sum of the hiring and attrition rates, leading to once again a negative and significant coefficient. All results provide strong evidence that both hiring and employee retention in these job categories declined with the start of the rise in U.S. protectionism in 2018.

Figure B2 in the Appendix provides additional insights into which types of jobs were most affected by the rise in protectionism. In Panel A, we show that, in terms of economic magnitude, the largest estimated effects were on the following job categories: Scientist (-8.55%), IT Project Manager (-5.58%), and Mechanical Engineer (-4.8%), based on Revelio's role_k50 classification. When using the role_k1000 classification within mechanical engineering roles, as shown in Panel B of Figure B2, the largest effects are estimated for Stress Engineer (-22.76%), Piping Designer (-16.61%), Design Engineer (-12.41%), Operations Engineer (-8.53%), Electrical Design Engineer (-7.86%), Technical Designer (-5.76%), and Mechanical Design Engineer (-5.55%), among others.

We also examine job postings for scientist and engineering roles by merging LinkUp's job postings database with Revelio's job categories.[21] Using this data, Appendix Table B3 shows an increase in active job postings in the U.S. for engineering and scientist roles, even after excluding software, IT, and data science jobs postings from our sample. This indicates that the decrease in U.S. scientists and engineers persists, despite firms actively seeking to hire for these roles.

Our results so far reveal a decrease in science and engineering positions at U.S. manufacturing firms following the start of U.S. protectionism. Further analysis indicates that this

[21] LinkUp dataset, previously utilized in recent studies (Campello et al., 2020; Cohen et al., 2020; Gutiérrez et al., 2020), contains 250+ million records from nearly 60,000 company websites, covering public and private entities globally. Each entry includes job location, employer details, key dates, and O*NET occupation codes. We match the O*NET occupation codes with Revelio's job categories using a linking table provided by Revelio.

reduction stems from fewer hirings rather than an increase in attrition. In fact, we find an overall decrease in turnover. These results are robust to looking at logged counts along with rates. Motivated by these findings, we next examine what drives the reduction in hiring. One wonders, for example, whether the reduction in hiring is due to changes in the entry of new employees in this sector or changes in the experienced ones.

[Table 6 about here]

Table 6 highlights a significant decrease in first-job employees (with a coefficient of -0.03, significant at the 1% level) and a statistically insignificant and economically small decrease in the hiring of experienced personnel. In line with this finding, we also observe a 2% reduction in junior positions and no significant change in mid-senior positions.

[Figure 6 about here]

Figure 6 provides evidence on the effect dynamics along with trends for treated and control units in the event time. It shows further evidence supporting the observable counterpart of the parallel trends assumption. There's a significant drop in the job categories affected, which makes up a big part of the observed changes. Overall, the figure highlights that companies aren't just shifting to hire more newcomers in non-technical positions; rather, they're actually hiring fewer science and engineering staff after the beginning of the era of U.S. protectionism. Figure B5 of the Appendix presents additional effect dynamics associated with other variables.

This section highlights key findings that demonstrate a reduction in science and engineering roles at U.S. chip manufacturing firms, mainly due to a decrease in new hires. The results presented here provide empirical evidence in line with the conceptual framework discussed in Section 3. In the next section, we address the potential impact of the concurrent increase in data science and programming roles on our estimates. We also take advantage of geographic variation within the labor force of U.S. chip manufacturing firms to provide an

economic mechanism with firms' H-1B visa exposures. Additionally, we investigate how the rise in U.S. protectionism affects the career paths of students with chip manufacturing skills. Specifically, we examine the number of students pursuing education in chip manufacturing and, among those who do, how many secure science and engineering roles compared to roles in alternative fields, such as marketing, operations, or finance.

5.2 Robustness: Disentangling Industry-Specific Effects from Broader Tech Trends

In this section, we provide robustness checks to our main results by excluding roles related to data science and programming. Remember that our primary analyses compare engineers and scientists to non-technical staff within each U.S. chip manufacturing firm in a given year, examining changes before and after the onset of protectionist policies in the U.S. The engineer and scientist positions include a broad spectrum of technical roles, including various engineering disciplines (e.g., manufacturing, automation, system test, mechanical), as well as technician roles (e.g., assembly, quality inspection, technical support) and R&D positions.

Within the engineer and scientist category, we recognize the presence of data science and software roles.[22] While these positions represent a minor fraction of the chip manufacturing workforce, their growing prominence coincident with U.S. protectionist policies demands careful consideration. For example, the reduction in the number of scientists and engineers could be driven by individuals leaving the chip manufacturing industry to work for data science or technology companies. To ensure the robustness of our findings, we conduct a targeted analysis of job titles, systematically identifying and excluding data science and programming roles.[23] This strategic exclusion serves a dual purpose: it allows us to isolate

[22]For example, we estimate a reduction of -5.58% in IT Project Manager roles in Appendix Figure B2.

[23]In particular, we search for job titles containing terms such as "data," "software," and "programming," which leads us to the following job titles: "advisory software engineer," "analyst programmer," "business data analyst," "clinical data," "computer programmer," "data analyst," "data architect," "data center," "data engineer," "data science," "data scientist," "database administrator," "database developer," "embedded software engineer," "java software developer," "oracle database administrator," "software architect," "software developer," "software engineer," "software quality assurance engineer," and "systems programmer."

the true impact of protectionist policies on core chip manufacturing roles, and it eliminates potential confounding effects from broader tech industry trends. By focusing on employees most likely to transition to data science and programming roles in other sectors, we effectively control for cross-industry labor flows. This refined approach strengthens our analysis, providing a more precise measure of protectionist policies' impact on the chip manufacturing workforce. We then re-estimate our regressions using this adjusted dataset, reinforcing the validity and specificity of our results.

[Table 7 about here]

As shown in Panel A of Table 7, the estimated effects on the logged number of scientists and engineers, as well as on hiring, separation, and turnover, remain economically and statistically significant. Importantly, these estimates closely align with those presented in Panel A of Table 5. Panels B and C of Table 7 further report estimates on employment growth rates and the heterogeneity of effects by career progression, which closely echo the estimates provided in Panel B of Table 5 and Table 6. These collective results reinforce the robustness of our findings presented in Section 5.1. They demonstrate that our main findings persist even when accounting for potential career transitions of data scientists and software engineers – the groups most prone to migrating to similar roles outside of the chip manufacturing industry. This consistency highlights the specific impact of protectionist policies on semiconductor workforce, distinct from broader tech sector trends.

6 Additional Findings: Mechanism and Effect Heterogeneity

This section will further deepen our empirical analyses by providing evidence for mechanism and effect heterogeneity. In Section 6.1, we analyze geographic variation in workforce dynamics among U.S. chip manufacturers in response to increased U.S. protectionist measures. This approach allows us to benchmark scientist and engineer roles at U.S. chip manufacturing firms in the U.S. against the same types of roles in different geographic segments of

the same firm within the same year. Then in Section 6.2, we study the influence of the H-1B ban on U.S. segments of U.S. chip manufacturers that rely on foreign labor. Then, we examine the role of tariff exposures in Section 6.3. Finally, in Section 6.4, we explore how protectionism influences the career trajectories of individuals educated alongside those with chip manufacturing skills.

6.1 Effect Heterogeneity by Location

We complement our main findings on the effect of protectionism on engineers and scientist in chip manufacturing in the U.S. by also examining how U.S. chip manufacturers change their workforce dynamics across the globe –i.e, at the country-job category-year level. This helps us shed light on whether the local (U.S.) segments drive the effects we estimate in Section 5.1 presenting our main findings. To do so, we first run regressions on

$$y_{i,c,j,t} = \omega \text{Treated}_j \times \text{Post}_t \times \text{US}_c + \alpha_{i,t} + \pi_{c,t} + \rho_{j,t} + \delta_{i,c,j} + \epsilon_{i,c,j,t}, \tag{10}$$

where i denotes the firm, c denotes country, j denotes the job category, and t represents the year. The dependent variables, $y_{i,j,t}$, are the same as the ones in Section **??**. The coefficient of interest in Equation (10) is ω, associated with $\text{Treated}_j \times \text{Post}_t \times \text{US}_c$. It quantifies the homogeneous average treatment effect of U.S. protectionism on science and engineering jobs at U.S. chip manufacturing firms within the United States.

On top of estimating the effect specifically in the U.S., the key advantage of Equation (10) is that it allows us to control for endogeneity at the job category-year level, which wasn't possible in Equation (9). When we drop $\rho_{j,t}$ from the specification, we also can and do estimate the effect of protectionism outside the United States, and present effect dynamics of both U.S. and non-U.S. effects within the same empirical model.

6.1.1 Findings: Global Workforce Dynamics of U.S. Chip Manufacturers

We present our findings in Table 8. In Panel A, the interaction term $\text{Treated}_j \times \text{Post}_t$, which denotes employment dynamics of American chip producers outside the United States, shows a slight increase in employment (2%, t-stat = 2.17). However, the triple interaction with US_c, which measures the differential effect of U.S. protectionism in U.S. segments of these firms, reveals a notable decline in employment within the United States (-5%, t-stat=4.76). In columns 2 to 8, we show that this reduction is driven by a decrease in hiring and it survives despite a decrease in separations. As shown, our results persist across various fixed effects structures, including firm-country-job category, firm-year, country-year, and notably, job category-year fixed effects.

[Table 8 about here]

The findings shown in Panel A corroborate the observations outlined in Section 5.1, highlighting a decline in overall employment of engineers and scientists by U.S. firms, primarily driven by reductions within the United States. Conversely, outside the United States, there's a minor increase in employee numbers. Panel B of Table 8 confirms that the findings from Panel A are robust to using rates rather than logged employee counts. Furthermore, the effect dynamics, as illustrated in Figure 7, show that pre-treatment employment trends for both U.S. and non-U.S. segments were parallel to those of their control units. There is a significant post-treatment decrease in scientist and engineer employment within the U.S., suggesting a distinct shift in employment strategies in post-2018 protectionist era.

[Figure 7 about here]

Panel C also presents important findings, underscoring that the increase in the number of employees in non-U.S. segments is at least partially driven by an increase in the number of experienced employees overseas. Specifically, there is a 3% increase in experienced overseas employees that take junior and mid-senior positions. This suggests a strategic focus on

enhancing workforce expertise in international segments. Columns 5 through 8 in Panel C further substantiate the results presented in Table 6, confirming the consistency and robustness of our findings across different specifications and approaches.

The primary objective of Table 8 is to utilize trends in non-U.S. segments as additional counterfactuals. This involves, for instance, comparing scientist and engineer counts of firms like Intel within the same fiscal year in the United States versus the ones in other geographic segment countries such as Canada and Mexico. To illuminate the effect of U.S. protectionism on each country, however, we perform subsample analyses. The outcomes of these analyses are shown in Figure B8 in the Appendix. As shown in this figure, U.S. chip manufacturers significantly expand their labor force in Canada, which strategically amended its immigration policies to welcome more foreign engineers and scientists in 2017, as well as in several European countries including the Netherlands.[24] Remarkably, 27.1% of the segment countries of U.S. chips firms in our sample exhibit a statistically significant positive effect. Of the remainder, 35.7% experience a positive yet insignificant effect, and 22.9% see a negative but insignificant effect. A combined total of 14.3% of the segment countries, including the U.S., experience a statistically significant negative impact.

[Table 9 about here]

6.2 Effect Heterogeneity by H-1B Sponsorship

Next, we examine the influence of the H-1B ban on U.S. segments of U.S. chip manufacturers, specifically focusing on firms that rely on foreign labor. We do so by running the regression model below, incorporating an additional interaction term into our triple difference

[24]Based on Esterline (2023) estimates, the U.S. lost 45,000 college grads to Canada's high-skill visa from 2017 to 2021.

framework in Equation (10).

$$
\begin{aligned}
y_{i,c,j,t} = \phi \text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i \\
+ \gamma \text{Treated}_j \times \text{Post}_t \times \text{US}_c \\
+ \eta \text{Treated}_j \times \text{Post}_t \times \text{Sponsor}_i \\
+ \theta \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i \\
+ \alpha_{i,t} + \pi_{c,t} + \rho_{j,t} + \delta_{i,c,j} + \epsilon_{i,c,j,t},
\end{aligned}
\tag{11}
$$

$Sponsor_i$ is equal to one for U.S. chip manufacturing firm i that sponsored H-1B petitions in fiscal year 2017 and zero otherwise. The coefficient of interest is ϕ, associated with the interaction term $Treated_j \times Post_t \times US_c \times Sponsor_i$, and γ from $Treated_j \times Post_t \times US_c$. ϕ estimates the influence of protectionist policies on the U.S. labor force of chip manufacturing firms that rely on foreign talent based on their recent H-1B sponsorship activity. The test shed light on the mechanism behind the decline in employment among U.S. manufacturers, emphasizing the significant adverse effects stemming from restricted labor access. According to Proposition 4, these effects are particularly pronounced in occupations that depend heavily on foreign labor and are characterized by a relatively inelastic labor supply. This, in turn, should predict a negative ϕ. In an alternative specification, we replace $Sponsor_i$ with $Log(Petitions_i)$, which reflects the number of H-1B petitions filed by firm i in 2017, allowing for analysis on the intensive margin.

Equation (11) also provides insights into the effect of protectionism on U.S. segments of firms that do not sponsor H-1B visas, captured by γ, on non-U.S. segments of firms that sponsor H-1B visas, represented by η, and on the non-engineering labor force in the U.S. for firms that sponsor H-1B visas, represented by θ. This approach allows us to provide a mechanism through which protectionism influences chip manufacturing workforce dynamics in the U.S., as discussed in Section 3.

6.2.1 Findings: H-1B Exposure and Workforce Dynamics

We present evidence on the influence of the H-1B ban on U.S. chip manufacturers using Equation (11) in Table 9. In Panel A, we estimate an 8% reduction in hires for firms that previously employed foreign workers before the H-1B ban. Panel B, column 1, supports this result when looking at the hiring rate instead of the total number of hires, while column 3 confirms a reduction in the net hiring rate, with decreases of 2% and 3%, respectively. These findings remain consistent when job category by year fixed effects are included, as shown in columns 5 to 9 in both panels. Overall, the results suggest that U.S. firms, which previously hired scientists and engineers through the H-1B visa program, have now reduced their hiring for these roles in the U.S. Panel C of Table 9 further shows that the H-1B ban has particularly affected hiring for non-entry-level positions, as these workers tend to have stronger qualifications compared to other workers in the chip manufacturing industry. Table B2 of the Appendix provides additional supporting evidence on the intensive margins.

The results presented in this section are important for three main reasons. First, from a statistical standpoint, we control for other layers of endogeneity by introducing geographic variation for each firm-year-job category. This approach allows us to implement more stringent fixed effect structures, enabling us to precisely estimate the effect of U.S. protectionism specifically on the employment of scientists and engineers within the United States. Second, we analyze how U.S. firms manage the risks and rewards associated with the rise of U.S. protectionism in 2018 by altering the geographic distribution of their workforce. We observe that these firms reduce hiring within the U.S.; however, given the global decline in student interest in acquiring chip manufacturing skills, U.S. firms appear to recruit more experienced workers outside the U.S. These individuals fill junior and mid-senior roles, which seem to be on the decline within the United States. Third, by examining H-1B exposure, we provide an economic mechanism driving our results.

6.3 Tariff Exposures

In this section, we examine how exposure to tariffs relate to scientist and engineering employment in the chip manufacturing industry. To do so, we employ tariff data from Fajgelbaum et al. (2020), who report U.S.-imposed tariffs on foreign countries at the 10-digit HS code level.[25] Our first step involves calculating the average maximum and scaled tariff rates by the HS-10 code and year. Our primary analysis focuses on tariffs as of 2018, considering that the post-2018 period is the post-treatment period in our analyses.

To calculate tariff exposure, we use the Pierce and Schott (2012) concordance tables, which provide a mapping between NAICS codes and HS-10 codes. This allows for useful industry-year level variation, as some NAICs codes are exposed to significantly more tariffs.[26] Based on this variation, we categorize industries into high and low tariff exposure groups. NAICS code 334413 represents the high-exposure category, which includes around half of our sample, while the remaining industries fall under low exposure (e.g., 333994, 334515, 333242, and 334418). Including the industry with the second-largest tariffs in the high-exposure group does not change our findings. We conduct regressions using specification (9) on these subsamples. Our theoretical framework suggests that higher tariffs on raw materials will lead to a monotonic decrease in equilibrium employment. Consequently, we examine the logged number of employees and net employee entry rate.

As shown in Table B5 in the Appendix, we observe statistically and economically significant reductions in scientist and engineering employment in the high tariff exposure group by 4% and 2%, respectively. Reductions in low tariff exposure industries are also significant, as expected due to indirect effects of tariffs and H-1B restrictions, but economically smaller: 2% and 1% reductions, respectively. These results align with our theoretical predictions,

[25] As an alternative approach, we also examine tariff rates specifically against China and get qualitatively similar results.

[26] For instance, NAICS code 334413 is subject to 45 different tariffs, while NAICS code 333242 is exposed to only 14. There is also heterogeneity in average scaled tariffs across industries: NAICS code 334413 has an average tariff exposure of 13.18% (averaged across matched HS-10 codes and countries in 2018), with a maximum average tariff of 24.4%, whereas NAICS code 334418 has a maximum tariff of 17.9% and an average tariff of 8.31%.

underscoring that reductions in scientist and engineering employment are more pronounced in industries with higher import tariff exposure. While we center our analysis on import tariffs, including retaliatory tariffs, which are available only at the HS-8 level, does not alter our primary findings.

6.4 Effects on Chip Manufacturing Talent

Our unique dataset allows us to track undergraduate and graduate classmates of employees with chip skills around the world. By analyzing these classmates, we can investigate the reasons behind the declines in both the count and rate of hiring in the semiconductor sector. Could these significant declines be attributed to reduced student interest in fields related to semiconductors? Are students with similar educational backgrounds now leaning towards other industries, such as finance and marketing, instead of chip manufacturing?

Panel C of Table 4 presents some summary statistics for cohorts, using 35,496 observations between 2014 and 2022 at the country-degree-job category-year level that capture the size of each cohort that take job type j after graduating from the same degree d from the same university in country c in year t, along with their average salary, seniority, and tenure in their first jobs, respectively. As shown, the average logged classmate size choosing job type j –Log(Cohort Size$_{c,d,j,t}$)– is equal to 1.21. While the average logged salary is equal to 6.02, the average seniority stands at 1.51, with a close median of 1.50, reflecting a relatively uniform early career progression among these individuals. Meanwhile, the tenure of these positions, Log(Tenure$_{c,d,j,t}$), has a mean (median) of 3.18 (5.02).

To explore how U.S. protectionism influences the entry of graduates into their first jobs in science and engineering fields, we track the career paths of individuals who graduated alongside those with chip manufacturing skills, within the same year, and who earned the same degree from the same university in the same country. Our goal is to analyze the career decisions of these peers in science and engineering jobs versus other fields, both before and after the protectionist era. To achieve this, we employ the below difference-in-differences

specification:

$$y_{c,d,j,t} = \tau \text{Treated}_j \times \text{Post}_t + \gamma_{c,d,j} + \theta_{c,t} + \zeta_{d,t} + \epsilon_{c,d,j,t}. \tag{12}$$

Our analysis focuses on $y_{c,d,j,t}$, a set of dependent variables capturing various labor market outcomes. Specifically, $\text{Log}(\text{Classmates}_{c,d,j,t})$ measures the number of individuals who, sharing the same graduation country (c), degree type (d) from the same university, and year (t), entered job category j alongside those with chip manufacturing skills. $\text{Log}(\text{Avg. Salary}_{c,d,j,t})$, $\text{Avg. Seniority}_{c,d,j,t}$, and $\text{Log}(\text{Tenure}_{c,d,j,t})$ detail the average salary, seniority level, and tenure duration of these classmates in their first jobs after graduation.

In specification (12), $Treated_j$ is assigned a value of one for science and engineering jobs, while it is equal to zero for finance, marketing, sales, operations, and administrative jobs. $Post_t$ takes a value of one for the years post-2018 and zero for the preceding years. We denote the disturbance term as $\epsilon_{c,d,j,t}$. The coefficient of interest in specification (12) is τ, which is associated with the interaction term $Treated_j \times Post_t$. This coefficient quantifies the homogeneous average treatment effect of protectionism on the number of science and engineering jobs taken by different educational cohorts—i.e., classmates of people with semiconductor skills—upon graduation.

To account for endogeneity, we incorporate a strong fixed effects structure, including country-degree-job category fixed effects ($\gamma_{c,d,j}$), country-year fixed effects ($\theta_{c,t}$), and degree-year fixed effects ($\zeta_{d,t}$). The country-degree-job category fixed effects help isolate variation at the country-degree-job category level, e.g. due to targeted government subsidies, while the country-year and degree-year fixed effects control for annual shocks specific to each country and degree, e.g. due to visa policies or educational trends. Once again, our key identifying assumption is parallel trends, and we support it by showcasing effect dynamics plots and trend plots for both treated and control job categories. We cluster standard errors at the country level to address potential serial correlation within countries.

6.4.1 Findings: Decreasing Interest in Science and Engineering Careers

Table 10 presents the changes in the number of classmates doing engineering and science jobs (Panel A), salaries (Panel B), seniority (Panel C), and length of first employment (Panel D) of the classmates of employees skilled in chips manufacturing post 2018. In each panel, we include country-job category-degree fixed effects. We also add year (in Column 1), country-year (in Column 2), degree-year (in Column 3), and finally both country-year and degree-year fixed effects (in Column 4). This table includes classmates from both undergraduate and graduate degrees.

[Table 10 about here]

Our difference-in-differences specification shows that, with the beginning of the high protectionism era in 2018, we see fewer number of the remaining classmates get engineering or scientist jobs. The coefficients in all four specifications of Panel A of Table 10 are negatively significant at the 1% level. The economic significance is high as well. We see 14–17% drop in the log number of classmates. The classmates of the talent in the chips industry, that skip engineering and science jobs, likely take finance, marketing or other higher paying jobs. Panel B shows the effect on their salaries. Classmates seem to have been enjoying not only higher salaries but also higher seniority (Panel C) post 2018.

As shown in Section B.1.5, our findings are robust to using a different dataset from the Department of Education on the number of graduate cohorts in the U.S. Our Revelio data aligns closely with the Department of Education data, with which we estimate a 14% decline in the number of graduates from bachelor and pre-bachelor degrees in the U.S. and a 15% decline in postgraduate degrees. Additionally, the reduction in the number of non-U.S. resident graduates is significant, amounting to near 17% and 29% in undergraduate and postgraduate programs. These findings are presented in Table B4 of the Appendix. Furthermore, additional untabulated results indicate a decline in the number of declared majors (in addition to degree completions) based on Department of Education data. These

results are available upon request.

Overall, our analysis reveals that, following the post-2018 era, there is a discernible decrease in the cohort sizes of students at both the undergraduate and graduate levels who are peers of individuals possessing chip manufacturing skills, indicating a waning interest in chip manufacturing industry within the U.S. Further investigation into those who remain within the same academic programs as individuals with chip manufacturing skills shows a tendency towards choosing careers outside of science and engineering.

7 Conclusion

Protectionist policies of the U.S. government starting in 2018 aimed to revive not only domestic manufacturing but also employment. Focusing on the semiconductor manufacturing, we ask whether these protectionist policies ended up protecting the key domestic talent. Unlike what was aimed, we see a significant decline in U.S. manufacturing firms' ability to attract not only international but also domestic talent with chip skills. Using a novel data set of 1.6 million employees with chip manufacturing skills worldwide, we find a reduction in domestic hiring, especially affecting entry-level and junior positions, in the U.S. chip manufacturing industry post 2018. Moreover, tracing job trajectories of undergraduate and graduate cohorts of workforce with chip manufacturing skills, we find significant shifts away from the chip industry. We observe that the talent educated with these skills, in fact, move to other countries or other industries post 2018.

Our findings carry significant implications for the 2021 Facilitating American-Built Semiconductors (FABS) Act and 2022 CHIPS and Science Act, which aim to bolster the U.S. semiconductor industry through extensive investments to enhance U.S. competitiveness globally. A Semiconductor Industry Association (SIA) report anticipates a significant expansion in the semiconductor workforce by 2030, with projections indicating a growth of nearly 115,000 jobs.[27] They also estimate that around 60% of these new positions, predominantly

[27]See https://bit.ly/3SDPD5j. Other forecasts indicate a projected shortfall of 300,000 engineers and

technical roles, may remain unfilled based on current degree completion rates. Our estimates suggest that unless measures are taken to address the labor shortage by attracting and retaining both domestic and international talent, the CHIPS Act may struggle to fully realize its objectives. Overcoming these challenges requires a nuanced approach that considers the complex interplay of trade policies, immigration reforms, and educational investments to ensure a skilled and sustainable workforce for the semiconductor industry.[28]

90,000 technical workers in our country by 2030. See https://bit.ly/3OTd35B.

[28]See the 'Chipmaker's Visa' for H-1B program: https://bit.ly/49dum9E.

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Table 1. **Active Chip Manufacturing Workforce**

This table shows the global distribution of employees, who possess skills in chip manufacturing and are actively employed as of March 2023. Panel A aggregates the total count of these employees across locations of employees and distributes them into various job categories (Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist), as defined by Revelio's clustering algorithms. *Total Emp.* refers to the total number employees with chip manufacturing skills. Panel B outlines employment characteristics for each country: *Tenure* is the average number of days active employees with chip manufacturing skills have spent in their current position; *RN* represents the average order of a job within an employee's career; *Salary* is the average annual income in USD; and *Seniority* refers to the average seniority level, categorized into seven levels. For more details on the data collection methodology and the definition of chip manufacturing skills, refer to Section B.1.1. For detailed variable definitions, please see Section B.2.

		Panel A: Employee Count by Job Category								Panel B: Economic Characteristics			
Rank	Country	Total Emp.	Admin	Engineer	Finance	Marketing	Operations	Sales	Scientist	Tenure	RN	Salary	Seniority
1	United States	680,602	26,373	480,193	8,531	11,578	31,790	72,622	49,515	2,819.03	5.47	100,384.72	2.95
2	India	165,352	9,880	122,978	2,476	2,728	7,216	11,946	8,128	1,986.43	4.11	12,750.81	2.79
3	United Kingdom	88,527	3,728	57,927	1,033	2,121	5,687	10,888	7,143	2,543.08	5.7	58,110.89	3.02
4	Canada	63,376	2,784	44,752	758	1,223	2,770	6,229	4,860	2,407.60	5.58	61,114.26	2.70
5	Germany	43,597	1,272	28,759	261	682	1,725	4,665	6,233	2,037.52	5.7	79,377.39	2.97
6	France	38,024	1,476	25,422	349	916	1,572	3,600	4,689	2,089.61	6.08	52,630.56	2.92
7	Italy	30,545	1,236	20,301	237	697	1,557	3,660	2,857	2,832.06	5.15	55,721.32	2.81
8	Australia	30,199	1,456	20,703	407	603	1,523	3,264	2,243	2,286.17	5.88	80,238.36	2.79
9	China	28,664	1,930	16,330	306	586	1,817	5,320	2,375	3,330.75	3.66	28,236.07	3.19
10	Netherlands	28,320	1,180	18,415	225	755	1,501	2,913	3,331	2,513.68	6.31	64,067.80	2.89
11	Brazil	25,968	1,999	17,787	466	497	1,415	2,396	1,408	2,711.02	5.48	14,588.81	2.51
12	Israel	21,956	572	16,511	103	275	889	1,516	2,090	2,395.99	4.99	73,976.56	3.16
13	Spain	20,989	1,166	14,450	176	493	724	1,708	2,272	2,413.65	5.62	50,341.81	2.72
14	Singapore	18,648	607	12,547	291	244	1,238	2,215	1,506	2,395.93	4.86	46,346.70	3.2
15	Pakistan	18,232	1,820	12,539	198	380	925	1,290	1,080	2,453.57	4.13	13,330.76	2.64
16	Mexico	18,137	843	13,291	175	260	1,237	1,464	867	2,643.00	5.01	29,523.58	2.79
17	Sweden	17,869	561	12,241	83	269	837	1,691	2,187	2,164.33	6.55	66,023.95	2.91
18	Turkey	16,575	885	11,537	125	290	589	1,626	1,523	2,034.55	5.02	20,327.08	2.69
19	Taiwan	16,312	565	10,919	142	221	960	2,320	1,185	3,233.21	3.86	76,870.21	3.25
20	Malaysia	13,874	706	10,613	168	141	730	948	568	2,654.82	4.13	21,392.26	2.85
	Other Countries	285,143	16,541	195,247	2,763	5,505	13,647	26,783	24,657	2,524.85	5.07	48,186.61	2.78

Table 2. **Top 25 Employers of Active Chip Manufacturing Workforce**

This table ranks the top 25 firms by the number of active employees around the globe with chip manufacturing skills as of March 2023. *Total Emp.* refers to the total number employees with chip manufacturing skills. *Seniority* is classified into seven levels, reflecting the hierarchical position within the company. In the case of multiple employers for a given employee, we keep the employer matching with the employee's highest job seniority. Further information on how data was gathered and the specific criteria used to identify chip manufacturing skills can be found in Section B.1.1. For detailed variable definitions, please see Section B.2.

			Seniority						
Rank	Employer	Total Emp.	1	2	3	4	5	6	7
1	Intel Corp.	29,178	1,268	15,397	3,658	3,787	4,344	697	27
2	Government of the USA	13,361	4,893	5,590	891	1,001	914	41	31
3	Apple, Inc.	11,956	449	7,589	1,259	1,177	1,382	96	4
4	Amazon.com, Inc.	10,976	327	4,115	1,677	2,325	2,188	338	6
5	QUALCOMM, Inc.	10,427	78	2,233	2,330	3,461	1,783	539	3
6	Siemens AG	9,063	540	3,977	1,618	1,551	1,203	153	21
7	Alphabet, Inc.	7,877	119	5,561	716	701	686	91	3
8	Raytheon Technologies Corp.	7,455	674	2,784	1,000	1,390	1,497	108	2
9	Advanced Micro Devices, Inc.	7,148	79	2,420	1,234	1,887	1,130	392	6
10	Microsoft Corp.	6,849	150	4,274	582	640	948	243	12
11	NXP Semiconductors NV	6,546	296	2,319	1,068	1,246	1,362	248	7
12	Robert Bosch Stiftung GmbH	6,457	523	3,819	740	658	587	124	6
13	Infineon Technologies AG	6,196	373	2,534	817	891	1,377	183	21
14	Texas Instruments Inc.	6,059	279	2,372	698	1,186	1,293	225	6
15	Samsung Electronics Co., Ltd.	5,996	395	2,615	580	666	1,520	213	7
16	Schneider Electric SE	5,560	572	2,532	727	810	771	138	10
17	Honeywell International, Inc.	5,434	593	3,064	489	609	586	85	8
18	STMicroelectronics NV	5,363	257	2,283	966	1,090	678	85	4
19	IBM Corp.	5,220	126	1,748	798	1,429	978	118	23
20	Analog Devices, Inc.	5,083	351	2,139	743	902	802	142	4
21	Broadcom, Inc.	5,076	159	1,537	647	802	1,799	127	5
22	NVIDIA Corp.	5,057	41	2,188	927	747	946	206	2
23	ABB Ltd.	4,960	378	2,313	693	809	703	57	7
24	Micron Technology, Inc.	4,883	236	1,260	595	1,056	1,427	302	7
25	Applied Materials, Inc.	4,693	163	1,343	680	936	1,236	316	19
	Other Employers	1,371,038	189,604	538,598	158,650	200,048	215,743	39,044	29,351

Table 3. **Industry Composition of Active Chip Manufacturing Workforce**

This table displays the industries employing the 680,602 active professionals in the U.S. with chip manufacturing skills. Panel A focuses on industries directly involved in chip manufacturing, while Panel B highlights the top 10 industries outside of chip manufacturing that also utilize U.S. chip manufacturing talent pool. *Total Emp.* refers to the total number employees with chip manufacturing skills. *Tenure* is the average number of days active employees with chip manufacturing skills have spent in their current position; *RN* represents the average order of a job within an employee's career; *Salary* is the average annual income in USD; and *Seniority* refers to the average seniority level, categorized into seven levels. For more details on the data collection methodology and the definition of chip manufacturing skills, refer to Section B.1.1. For detailed variable definitions, please see Section B.2.

Panel A: Chip Manufacturing Industries

Rank	Industry	NAICS	Total Emp.	Tenure	RN	Salary	Seniority
1	Semiconductor and Related Device Manufacturing	334413	72,512	3,035.24	4.9	113,197.25	3.24
2	Semiconductor Machinery Manufacturing	333242	7,943	3,159.26	4.99	109,462.64	3.34
3	Instrument Mfg. for Electricity & Electrical Signal Testing	334515	6,514	3,719.29	4.73	101,481.78	2.97
4	Printed Circuit Assembly (Electronic Assembly) Manufacturing	334418	1,526	4,054.05	4.32	98,851.70	3.16

Panel B: Other Industries

Rank	Industry	NAICS	Total Emp.	Tenure	RN	Salary	Seniority
1	Software Publishers	511210	35,572	1,811.93	6.42	122,691.03	3.22
2	Colleges, Universities, and Professional Schools	611310	27,661	2,905.84	5.3	78,354.48	2.46
3	Radio/TV Broadcasting & Wireless Communications Equipment Mfg.	334220	14,591	2,227.03	5.55	125,834.12	2.8
4	Internet Publishing and Broadcasting and Web Search Portals	519130	13,512	1,270.00	6.67	136,641.06	2.74
5	Search & Navigation System Instrument Mfg.	334511	12,868	2,978.82	5.28	96,177.27	2.72
6	Other Computer Related Services	541519	10,877	2,421.91	5.89	109,739.59	3.34
7	Engineering Services	541330	10,593	2,565.56	5.4	94,665.02	2.67
8	Surgical and Medical Instrument Manufacturing	339112	9,991	2,822.09	5.69	102,990.94	3.17
9	Other Electronic Component Manufacturing	334419	9,230	3,534.28	4.82	98,744.39	3.03
10	Automobile Manufacturing	336111	8,664	2,253.57	5.92	93,032.16	2.74

Table 4. **Summary Statistics**

This table provides a detailed overview of the variables utilized in our empirical analysis. Panel A offers summary statistics related to U.S. chip manufacturing firms, Panel B presents these at the geographic segment level, while Panel C focuses on classmates of individuals with chip manufacturing skills. These classmates are defined as students who graduated with the same degree, from the same university, in the same country, and year. For detailed information on data collection methods and detailed definitions of the variables, please see Sections B.1.3, B.1.4, and B.2.

Panel A: U.S. Chip Manufacturer Workforce						
	N	Mean	Median	SD	P5	P95
$\text{Log(Emp}_{i,j,t}\text{)}$	68,949	1.76	1.39	1.47	0.00	4.86
$\text{Log(Hiring}_{i,j,t}\text{)}$	68,949	0.62	0.00	0.96	0.00	2.89
$\text{Log(Separation}_{i,j,t}\text{)}$	68,949	0.59	0.00	0.92	0.00	2.77
$\text{Log(Turnover}_{i,j,t}\text{)}$	68,949	0.88	0.69	1.16	0.00	3.50
$\text{Hiring Rate}_{i,j,t}$	56,497	0.16	0.00	0.38	0.00	0.83
$\text{Separation Rate}_{i,j,t}$	56,497	0.12	0.00	0.22	0.00	0.50
$\text{Net Hiring Rate}_{i,j,t}$	56,497	0.04	0.00	0.38	-0.33	0.50
$\text{Turnover Rate}_{i,j,t}$	56,497	0.28	0.14	0.49	0.00	1.00
$\text{Log(FirstJobEmp}_{i,j,t}\text{)}$	68,949	0.95	0.69	1.23	0.00	3.50
$\text{Log(ExprEmp}_{i,j,t}\text{)}$	68,949	1.56	1.10	1.52	0.00	4.60
$\text{Log(JunPosEmp}_{i,j,t}\text{)}$	68,949	1.45	1.10	1.50	0.00	4.47
$\text{Log(MidSenPosEmp}_{i,j,t}\text{)}$	68,949	1.04	0.69	1.29	0.00	3.66
Panel B: Regional U.S. Chip Manufacturer Workforce						
	N	Mean	Median	SD	P5	P95
$\text{Log(Emp}_{i,c,j,t}\text{)}$	231,696	1.24	0.69	1.24	0.00	3.83
$\text{Log(Hiring}_{i,c,j,t}\text{)}$	231,696	0.36	0.00	0.72	0.00	2.08
$\text{Log(Separation}_{i,c,j,t}\text{)}$	231,696	0.33	0.00	0.67	0.00	1.79
$\text{Log(Turnover}_{i,c,j,t}\text{)}$	231,696	0.53	0.00	0.89	0.00	2.56
$\text{Hiring Rate}_{i,c,j,t}$	166,411	0.12	0.00	0.27	0.00	0.75
$\text{Separation Rate}_{i,c,j,t}$	166,411	0.10	0.00	0.22	0.00	0.50
$\text{Net Hiring Rate}_{i,c,j,t}$	166,411	0.01	0.00	0.29	-0.46	0.50
$\text{Turnover Rate}_{i,c,j,t}$	166,411	0.23	0.00	0.39	0.00	1.00
$\text{Log(FirstJobEmp}_{i,c,j,t}\text{)}$	231,696	0.60	0.00	0.86	0.00	2.40
$\text{Log(ExprEmp}_{i,c,j,t}\text{)}$	231,696	1.02	0.69	1.20	0.00	3.58
$\text{Log(JunPosEmp}_{i,c,j,t}\text{)}$	231,696	0.98	0.69	1.15	0.00	3.43
$\text{Log(MidSenPosEmp}_{i,c,j,t}\text{)}$	231,696	0.65	0.00	0.93	0.00	2.71
Panel C: Educational Cohorts of Chip Manufacturing Employees						
	N	Mean	Median	SD	P5	P95
$\text{Log(Classmates}_{c,d,j,t}\text{)}$	35,496	1.21	0.69	1.56	0.00	4.44
$\text{Log(Avg. Salary}_{c,d,j,t}\text{)}$	35,496	6.02	9.42	5.14	0.00	11.29
$\text{Avg. Seniority}_{c,d,j,t}$	35,496	1.51	1.50	1.56	0.00	4.33
$\text{Log(Tenure}_{c,d,j,t}\text{)}$	35,496	3.18	5.02	2.79	0.00	6.19

Table 5. **Science and Engineering Employment in U.S. Chip Manufacturing Companies**

This table presents our findings on how U.S. protectionism has influenced science and engineering employment at U.S. chip manufacturing companies. Utilizing the difference-in-differences approach outlined in Equation (9), we analyze the effects on employment metrics. Panel A shows the effects on employee count, hiring practices, separation, and turnover, while Panel B focuses on these metrics in rate form instead of logged numbers. We set missing rate variables to zero and control for them with an untabulated dummy variable. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.09***	-0.04***	-0.09***
	(-3.45)	(-8.93)	(-4.19)	(-7.73)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.975	0.874	0.863	0.889
Panel B: Analyses of Employment Growth				
	$\text{Hiring Rate}_{i,j,t}$	$\text{Separation Rate}_{i,j,t}$	$\text{Net Hiring Rate}_{i,j,t}$	$\text{Turnover Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.01***	-0.02***	-0.04***
	(-4.70)	(-3.54)	(-3.16)	(-5.16)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.393	0.390	0.342	0.421

Table 6. **Science and Engineering Employment by Career Progression**

This table presents the impact of U.S. protectionism on science and engineering employment within U.S. chip manufacturing companies, segmented by experience and seniority. Utilizing the difference-in-differences methodology outlined in Equation (9), column 1 shows the number of employees hired for the first time, and column 2 focuses on employees with prior work experience. Columns 3 and 4 present results from categorizing employees based on seniority. For details on data collection and variable definitions, see Sections B.1.3 and B.2. The analysis, covering 2014 to 2022, uses firm-level clustered standard errors. Statistical significance at 1%, 5%, and 10% levels is indicated by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.01	-0.02**	-0.01
	(-4.27)	(-1.55)	(-2.04)	(-0.81)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,949	68,949	68,949	68,949
R-squared	0.983	0.974	0.974	0.973

Table 7. **Main Findings After Excluding Data Science and Programming Roles**

This table presents our main findings after excluding all data and programming related roles at U.S. chip manufacturing companies, as explained in Section 6.4.1. Panel A shows the effects on employee count, hiring, separation, and turnover, and Panel B focuses on these metrics in rate form instead of logged numbers. Panel C presents our findings by career progression. We set missing rate variables to zero and control for them with an untabulated dummy variable. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.08***	-0.04***	-0.08***
	(-3.51)	(-8.46)	(-4.10)	(-7.52)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,886	68,886	68,886	68,886
R-squared	0.975	0.872	0.861	0.887
Panel B: Analyses of Employment Growth				
	Hiring $\text{Rate}_{i,j,t}$	Separation $\text{Rate}_{i,j,t}$	Net Hiring $\text{Rate}_{i,j,t}$	Turnover $\text{Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.01***	-0.02***	-0.04***
	(-4.55)	(-3.64)	(-2.86)	(-5.08)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,886	68,886	68,886	68,886
R-squared	0.395	0.390	0.343	0.422
Panel C: Analyses of Chip Manufacturing Workforce by Career Progression				
	$\text{Log}(\text{FirstJobEmp}_{i,j,t})$	$\text{Log}(\text{ExprEmp}_{i,j,t})$	$\text{Log}(\text{JunPosEmp}_{i,j,t})$	$\text{Log}(\text{MidSenPosEmp}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.03***	-0.02	-0.02**	-0.01
	(-4.46)	(-1.64)	(-2.09)	(-0.99)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,886	68,886	68,886	68,886
R-squared	0.983	0.973	0.974	0.973

Table 8. **Effect Heterogeneity: U.S. vs. Non-U.S. Workforce Dynamics**

This table presents our findings on how U.S. protectionism has influenced the geography of science and engineering employees at U.S. chip manufacturing companies. Utilizing the difference-in-differences approach outlined in Equation (10), Panel A presents the effects on employee count, hiring practices, separation, and turnover, Panel B focuses on these metrics in rate form instead of absolute numbers, and Panel C focuses on metrics by career progression. We set missing rate variables to zero and control for them with an untabulated dummy variable. *FirstJobEmp*, *JunPosEmp* and *MidSenPosEmp* are shortened to *FirstEmp*, *JunEmp* and *MidSenEmp* for brevity. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Analyses of Chip Manufacturing Workforce (N=231,696)								
	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.05***	-0.07***	-0.04***	-0.07***	-0.05***	-0.07***	-0.04***	-0.06***
	(-4.76)	(-4.92)	(-3.23)	(-4.21)	(-4.74)	(-4.71)	(-3.12)	(-4.00)
$\text{Treated}_j \times \text{Post}_t$	0.02**	-0.03**	-0.01	-0.04**				
	(2.17)	(-2.39)	(-1.00)	(-2.28)				
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes
R-squared	0.948	0.781	0.760	0.806	0.948	0.781	0.760	0.807
Panel B: Analyses of Employment Growth (N=231,696)								
	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01***	-0.01***	-0.01**	-0.02***	-0.01***	-0.01**	-0.01**	-0.02***
	(-3.83)	(-2.68)	(-2.62)	(-3.88)	(-3.60)	(-2.64)	(-2.40)	(-3.72)
$\text{Treated}_j \times \text{Post}_t$	-0.01***	-0.00	-0.01**	-0.02***				
	(-4.03)	(-1.43)	(-2.62)	(-3.46)				
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes
R-squared	0.329	0.281	0.211	0.349	0.329	0.281	0.212	0.350
Panel C: Analyses of Chip Manufacturing Workforce by Career Progression (N=231,696)								
	$\text{Log(FirstEmp}_{i,c,j,t})$	$\text{Log(ExprEmp}_{i,c,j,t})$	$\text{Log(JunEmp}_{i,c,j,t})$	$\text{Log(MidSenEmp}_{i,c,j,t})$	$\text{Log(FirstEmp}_{i,c,j,t})$	$\text{Log(ExprEmp}_{i,c,j,t})$	$\text{Log(JunEmp}_{i,c,j,t})$	$\text{Log(MidSenEmp}_{i,c,j,t})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01***	-0.06***	-0.04***	-0.03***	-0.01***	-0.06***	-0.05***	-0.03***
	(-2.69)	(-4.90)	(-4.23)	(-3.15)	(-2.90)	(-4.88)	(-4.28)	(-3.15)
$\text{Treated}_j \times \text{Post}_t$	-0.01	0.03***	0.02**	0.02**				
	(-1.51)	(3.04)	(2.10)	(2.36)				
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes
R-squared	0.961	0.940	0.943	0.939	0.961	0.940	0.943	0.939

Table 9. **Effect Heterogeneity: U.S. vs. Non-U.S. Workforce and the Role of H-1B Hiring**

This table reports our estimates of the heterogeneous effect of U.S. protectionism on workforce dynamics in U.S. chip manufacturing firms, both domestically and internationally, as well as among firms that rely on foreign talent and those that do not. The results are based on Equation (11). Sponsor_i indicates whether firm i sponsored H1B petitions in fiscal year 2017 based on USCIS's H-1B Employer Data Hub. The remaining variables are explained in Table 8. The analysis spans the years 2014 to 2022, utilizing clustered standard errors by firm. Statistical significance at 1%, 5%, and 10% levels are indicated by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

	Panel A: Analyses of Chip Manufacturing Workforce (N=231,696)							
	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$	$\text{Log(Emp}_{i,c,j,t})$	$\text{Log(Hiring}_{i,c,j,t})$	$\text{Log(Separation}_{i,c,j,t})$	$\text{Log(Turnover}_{i,c,j,t})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.03	-0.08***	-0.03*	-0.06**	-0.03	-0.09***	-0.03*	-0.06**
	(-1.54)	(-4.09)	(-1.79)	(-2.47)	(-1.54)	(-4.09)	(-1.79)	(-2.47)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.03***	-0.05***	-0.02	-0.04***	-0.03***	-0.04***	-0.01	-0.04**
	(-2.93)	(-4.14)	(-1.51)	(-2.66)	(-2.94)	(-3.87)	(-1.41)	(-2.43)
$\text{Treated}_j \times \text{Post}_t \times \text{Sponsor}_i$	0.05**	0.02	0.06***	0.07***	0.05**	0.02	0.06***	0.07***
	(2.53)	(0.97)	(3.47)	(2.72)	(2.54)	(1.00)	(3.49)	(2.75)
$\text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.02	-0.01	0.02	0.01	-0.02	-0.01	0.02	0.01
	(-1.03)	(-0.50)	(0.69)	(0.37)	(-1.00)	(-0.48)	(0.70)	(0.39)
$\text{Treated}_j \times \text{Post}_t$	-0.00	-0.04***	-0.04***	-0.07***				
	(-0.01)	(-3.68)	(-3.42)	(-4.51)				
R-squared	0.948	0.781	0.760	0.807	0.948	0.781	0.760	0.807
	Panel B: Analyses of Employment Growth (N=231,696)							
	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.02***	0.01	-0.03***	-0.01	-0.02***	0.01	-0.03***	-0.01
	(-2.80)	(1.49)	(-4.28)	(-1.18)	(-2.80)	(1.48)	(-4.27)	(-1.19)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01*	-0.01***	-0.00	-0.02**	-0.01	-0.01***	-0.00	-0.01**
	(-1.78)	(-2.77)	(-0.56)	(-2.48)	(-1.59)	(-2.72)	(-0.39)	(-2.34)
$\text{Treated}_j \times \text{Post}_t \times \text{Sponsor}_i$	0.01	0.00	0.01	0.01	0.01	0.00	0.01	0.01
	(0.77)	(0.62)	(0.77)	(0.75)	(0.81)	(0.63)	(0.81)	(0.78)
$\text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.00	-0.00	0.00	-0.01	-0.00	-0.00	0.00	-0.01
	(-0.55)	(-1.01)	(0.01)	(-0.89)	(-0.53)	(-1.00)	(0.03)	(-0.87)
$\text{Treated}_j \times \text{Post}_t$	-0.02***	-0.00*	-0.01***	-0.02***				
	(-3.67)	(-1.80)	(-2.77)	(-3.36)				
R-squared	0.329	0.281	0.211	0.349	0.329	0.281	0.212	0.350
	Panel C: Analyses of Chip Manufacturing Workforce by Career Progression (N=231,696)							
	$\text{Log(FirstEmp}_{i,c,j,t})$	$\text{Log(ExprEmp}_{i,c,j,t})$	$\text{Log(JunEmp}_{i,c,j,t})$	$\text{Log(MidSenEmp}_{i,c,j,t})$	$\text{Log(FirstEmp}_{i,c,j,t})$	$\text{Log(ExprEmp}_{i,c,j,t})$	$\text{Log(JunEmp}_{i,c,j,t})$	$\text{Log(MidSenEmp}_{i,c,j,t})$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.02*	-0.05**	-0.02	-0.04**	-0.02*	-0.05**	-0.02	-0.04**
	(-1.83)	(-2.04)	(-1.03)	(-2.52)	(-1.82)	(-2.04)	(-1.04)	(-2.52)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01	-0.03**	-0.03***	-0.01	-0.01*	-0.03**	-0.03***	-0.01
	(-1.65)	(-2.56)	(-2.86)	(-1.01)	(-1.89)	(-2.57)	(-2.94)	(-1.02)
$\text{Treated}_j \times \text{Post}_t \times \text{Sponsor}_i$	0.01	0.06***	0.04**	0.05***	0.01	0.06***	0.04**	0.05***
	(0.77)	(2.90)	(2.05)	(3.15)	(0.76)	(2.91)	(2.05)	(3.17)
$\text{Post}_t \times \text{US}_c \times \text{Sponsor}_i$	-0.01	-0.02	-0.03	0.02	-0.01	-0.02	-0.03	0.02
	(-0.77)	(-0.98)	(-1.46)	(0.78)	(-0.75)	(-0.96)	(-1.44)	(0.80)
$\text{Treated}_j \times \text{Post}_t$	-0.01**	0.01	0.00	-0.00				
	(-2.07)	(0.54)	(0.25)	(-0.19)				
R-squared	0.961	0.940	0.943	0.939	0.961	0.940	0.943	0.939
	Panel D: Controls for Panels A, B, and C							
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes

Table 10. **Career Choices of Students Graduating with Chip Manufacturing Skills**

This table presents our findings on the effect of U.S. protectionism on the unique number of students who complete their education equipped with relevant skills in chip manufacturing and find jobs. To pinpoint these students, we identify the peers of individuals with chip manufacturing skills who graduated in the same year, pursued the same degree at the same university of the same country. We then examine these peers' career choices both before and after the beginning of U.S. protectionism in 2018. We use the difference-in-differences methodology outlined in Equation (12). In Panel A, we display the number of peers who secured initial jobs in various job categories, distinguishing between science and engineering positions and other categories. Panel B provides information on the salaries of peers in different job categories. Panels C and D analyze the starting seniority levels and tenure, which measures the number of days these peers work in their first jobs across different job categories after graduating with the same degree, year, and country as those with chip manufacturing skills. For detailed insights into data collection and variable definitions, please refer to Sections B.1.4 and B.2. Our analysis spans the period from 2014 to 2022 and employs country-level clustered standard errors. Statistical significance at 1%, 5%, and 10% levels is indicated by $\star\star\star$, $\star\star$, and $\star$, respectively.

Panel A: Regressions of Log(Classmates$_{c,d,j,t}$)				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	-0.14***	-0.15***	-0.14***	-0.17***
	(-11.92)	(-13.61)	(-11.63)	(-14.10)
Observations	35,496	35,424	35,496	35,424
R-squared	0.940	0.950	0.945	0.956
Panel B: Regressions of Log(Salary$_{c,d,j,t}$)				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	0.03***	0.03***	0.04***	0.04***
	(3.05)	(3.06)	(3.48)	(3.51)
Observations	35,496	35,424	35,496	35,424
R-squared	0.994	0.995	0.994	0.995
Panel C: Regressions of Seniority$_{c,d,j,t}$				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	0.11***	0.10***	0.11***	0.11***
	(6.47)	(6.28)	(7.00)	(6.86)
Observations	35,496	35,424	35,496	35,424
R-squared	0.769	0.780	0.770	0.781
Panel D: Regressions of Log(Tenure$_{c,d,j,t}$)				
	(1)	(2)	(3)	(4)
Treated$_j$ × Post$_t$	0.02	0.02	0.02	0.00
	(1.59)	(1.14)	(0.98)	(0.25)
Observations	35,496	35,424	35,496	35,424
R-squared	0.943	0.946	0.943	0.947
Panel E: Controls for Panels A, B, C, and D				
	(1)	(2)	(3)	(4)
Country × Job Category × Degree FE	Yes	Yes	Yes	Yes
Year FE	Yes	No	No	No
Country × Year FE	No	Yes	No	Yes
Degree × Year FE	No	No	Yes	Yes

Figure 1. **Active Employees with Chip Manufacturing Skills**

This figure illustrates the global distribution of employees with chip manufacturing skills who are actively employed as of March 2023. Methodological details and definitions regarding chip manufacturing skills are available in Section B.1.1.

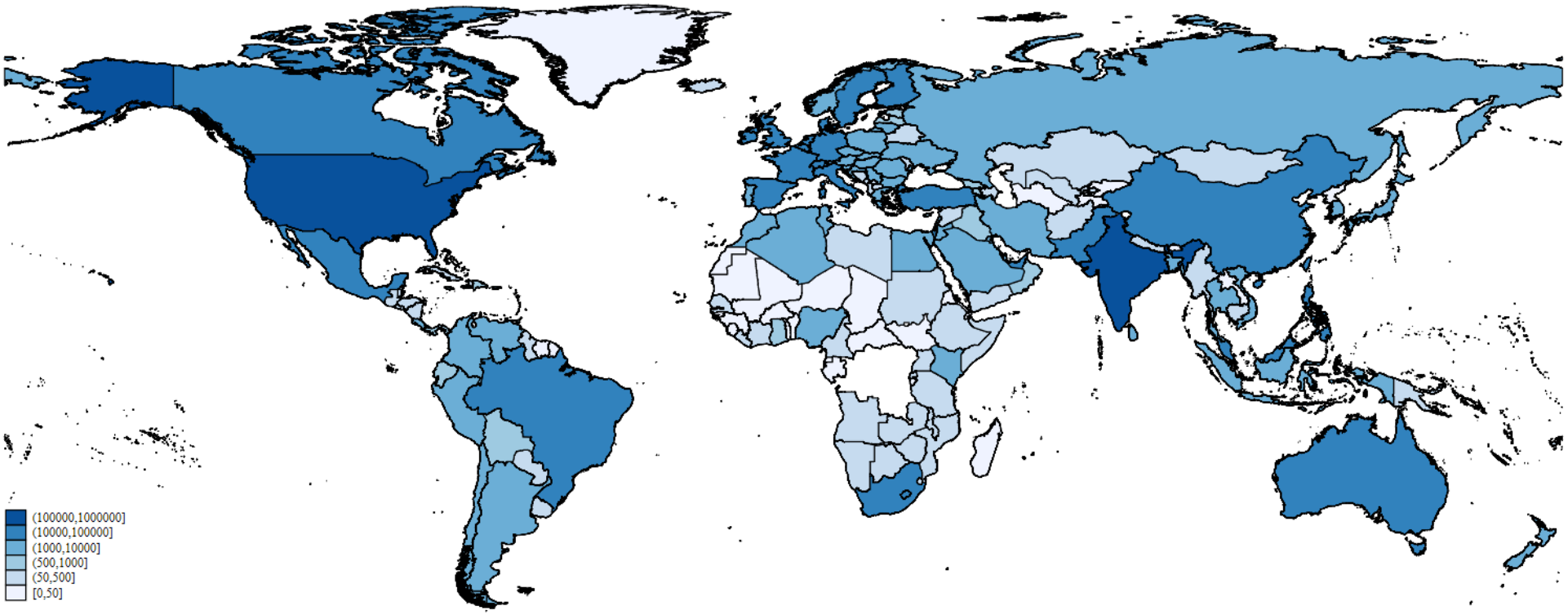


Figure 2. **US Share of Chip Manufacturing Skills**

This figure presents the list of skills utilized to identify individuals with chip manufacturing expertise, alongside the percentage representation of each skill among employees in the US. Methodological details and definitions regarding chip manufacturing skills are available in Section B.1.1.

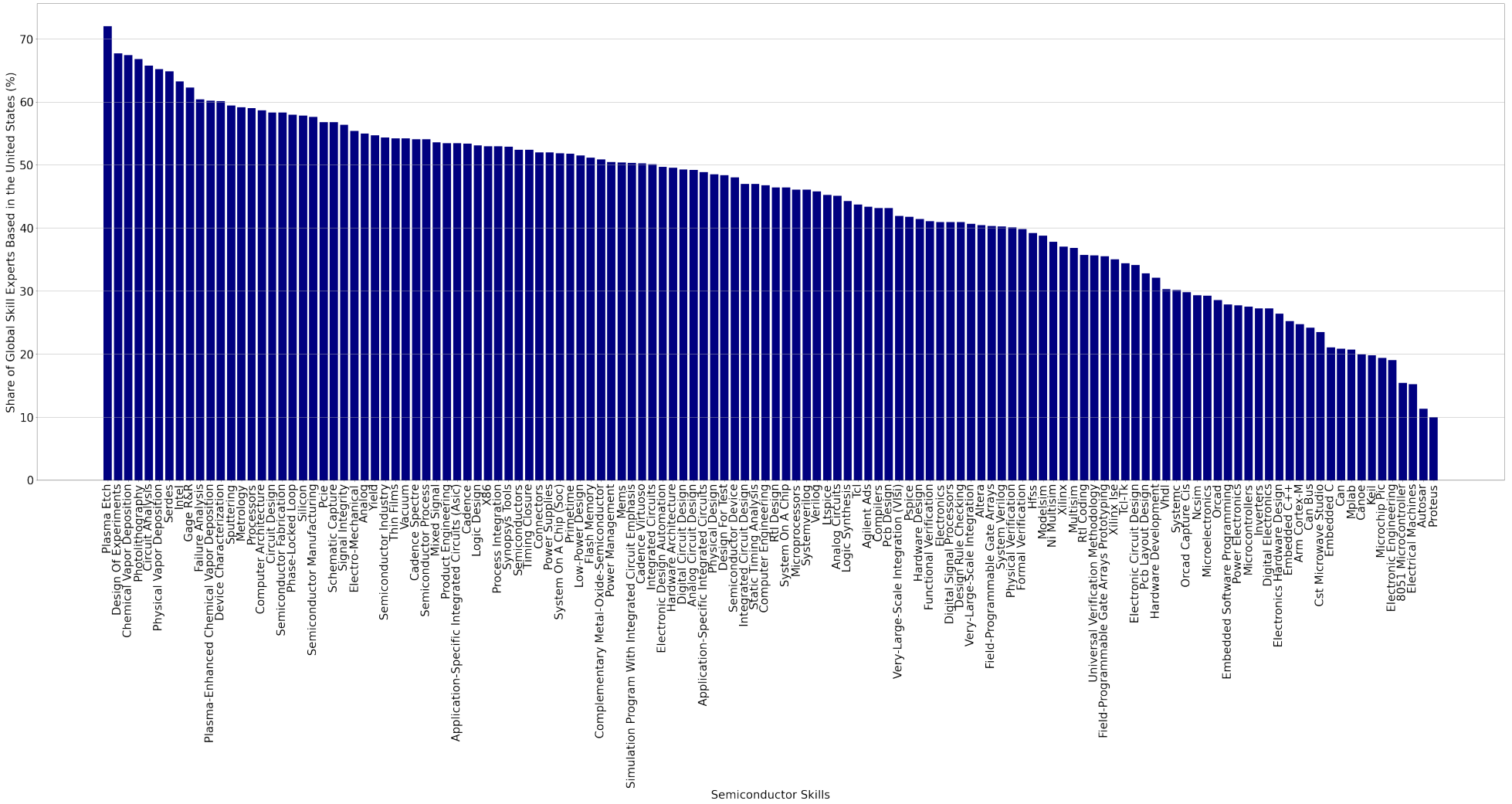


Figure 3. **Total Employment by Job Category in U.S. Chip Manufacturing Firms**

This figure displays the aggregate number of employees categorized by job descriptions at U.S. chip manufacturing firms as of the end of 2017. We do not display categories with fewer than 1,000 observations for readability. For detailed methodological information and definitions related to chip manufacturing skills, please refer to Section B.1.3.

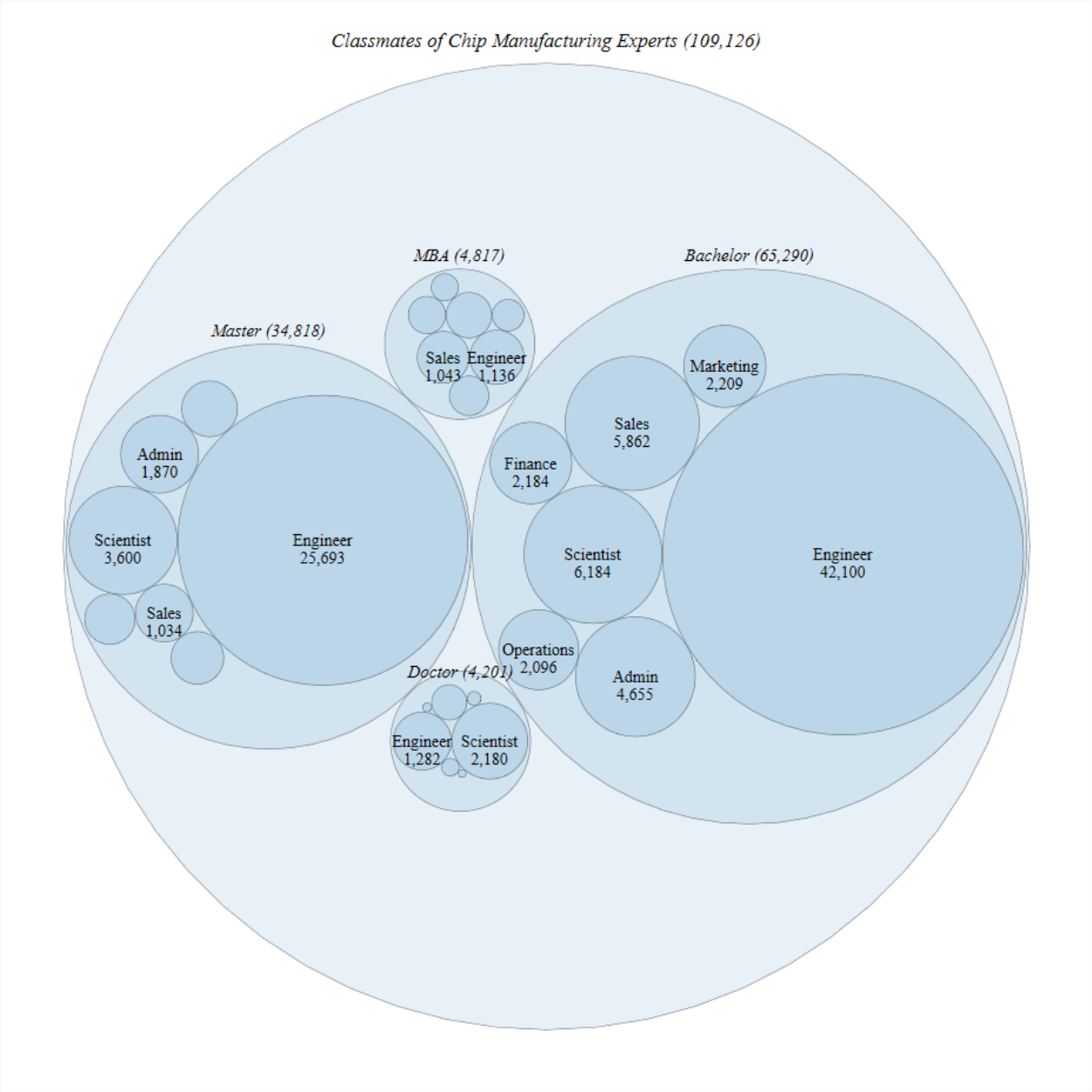


Figure 4. **Total Employment by Job Category in U.S. Chip Manufacturing Firms**

This figure displays the aggregate number of employees categorized by job descriptions at U.S. chip manufacturing firms as of the end of 2017. For detailed methodological information and definitions related to chip manufacturing skills, please refer to Section B.1.3.

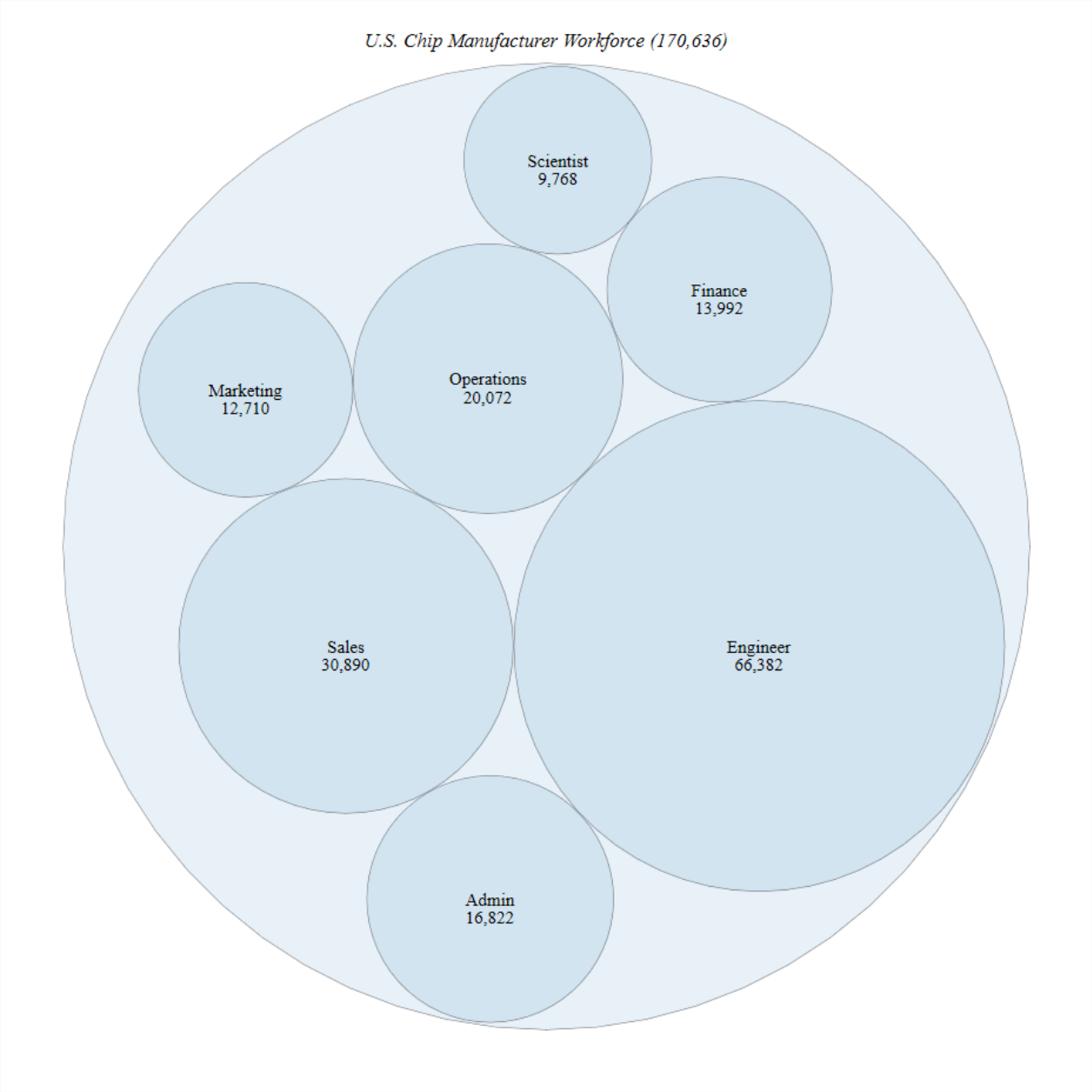


Figure 5. **Effect Dynamics: Science and Engineering Positions at U.S. Chip Manufacturers**

The initial figure illustrates the time-varying effects of U.S. protectionism on the logarithm of the number of employees in engineering and science roles. These effects are calculated using a difference in differences model as in specification (9), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. The second figure displays the fitted trend comparisons between the treated group (employees in engineering and science) and the control group (employees in administration, finance, marketing, operations, and sales) employees of the same firm in the same year. In these trend analyses, data are adjusted by removing the effects of firm × job category, as well as year fixed effects. See Section 5.1 for more details on this methodology. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively.

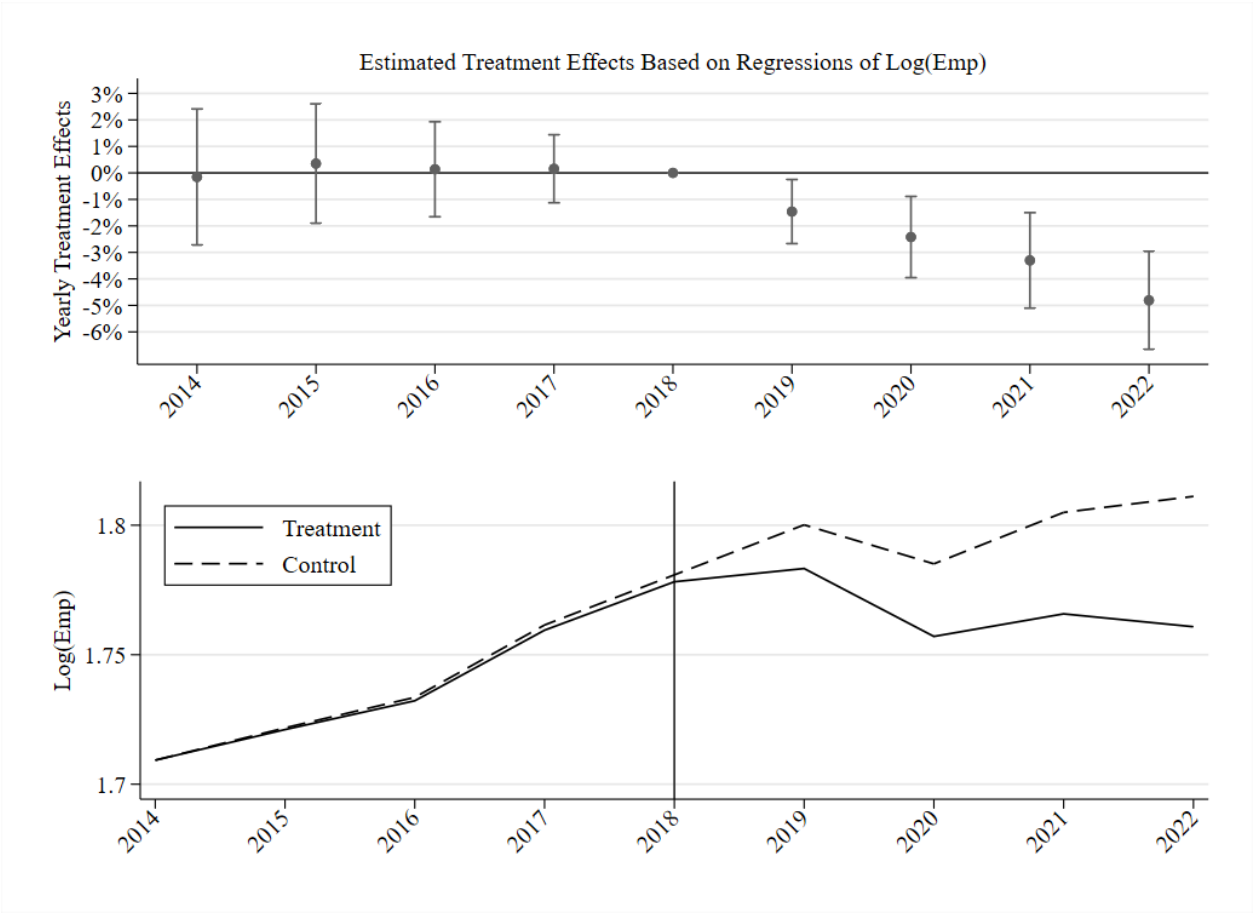


Figure 6. **Effect Dynamics: First Science and Engineering Jobs at U.S. Chip Manufacturers**

The initial figure illustrates the time-varying effects of U.S. protectionism on the logarithm of the number of first-job employees in engineering and science roles. These effects are calculated using a difference in differences model as in specification (9), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. The second figure displays the trend comparisons between the treated group (employees in engineering and science) and the control group (employees in administration, finance, marketing, operations, and sales) employees of the same firm in the same year. In these trend analyses, data are adjusted by removing the effects of firm × job category, as well as year fixed effects. See Section 5.1 for more details on this methodology. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively.

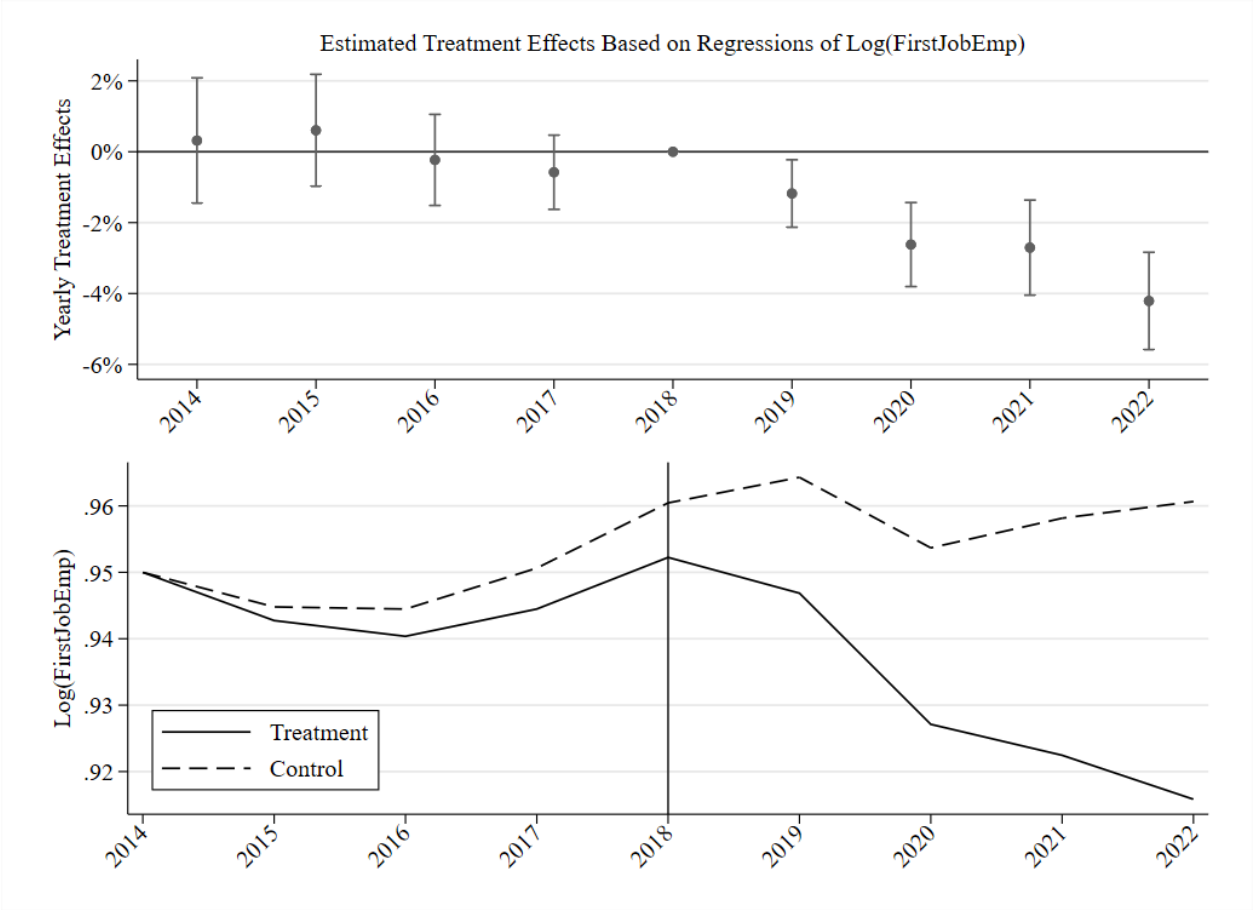


Figure 7. **Effect Dynamics: Global Workforce Trends in U.S. Chip Manufacturers**

The figure illustrates the dynamic effect of U.S. protectionist policies on the logarithmic scale of employment counts in science and engineering positions, both within (represented by orange squares) and outside (represented by blue triangles) the United States. This analysis is conducted using a difference-in-differences approach as outlined in specification (10), accounting for interactions between firm, country, and job category, as well as firm × year and country × year fixed effects. Each point estimate is accompanied by a 95% confidence interval. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively.

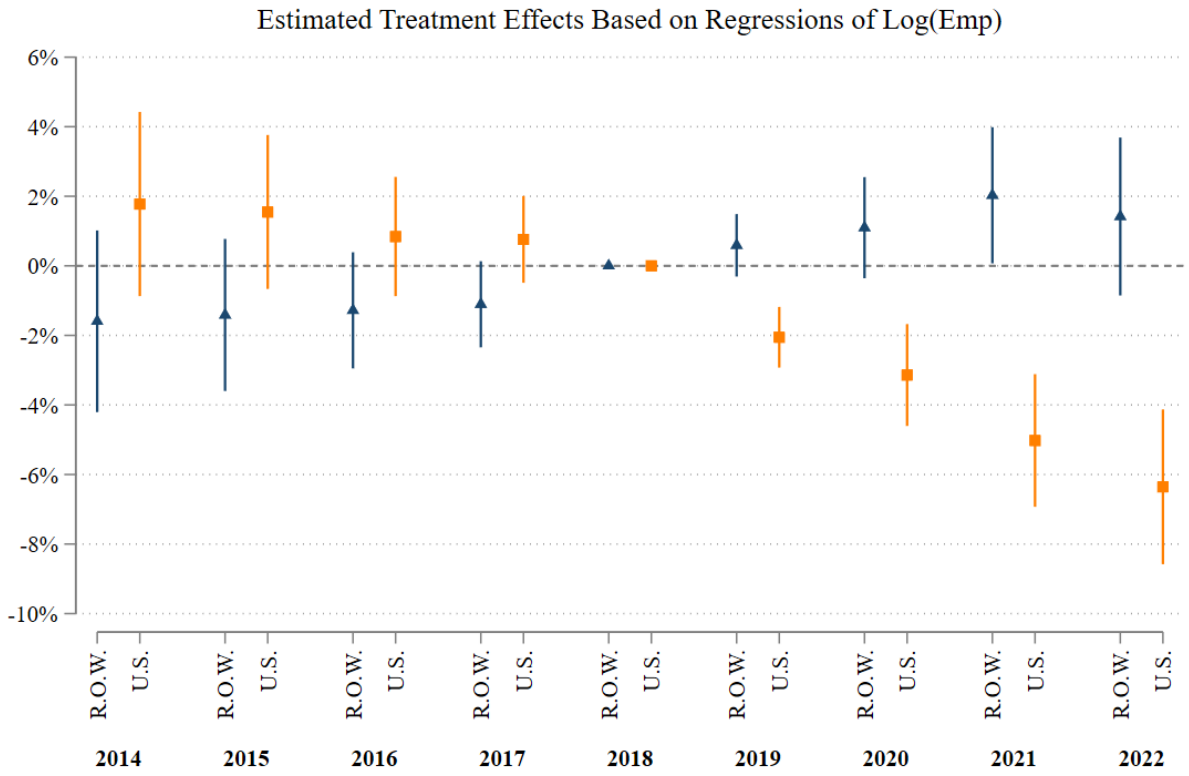
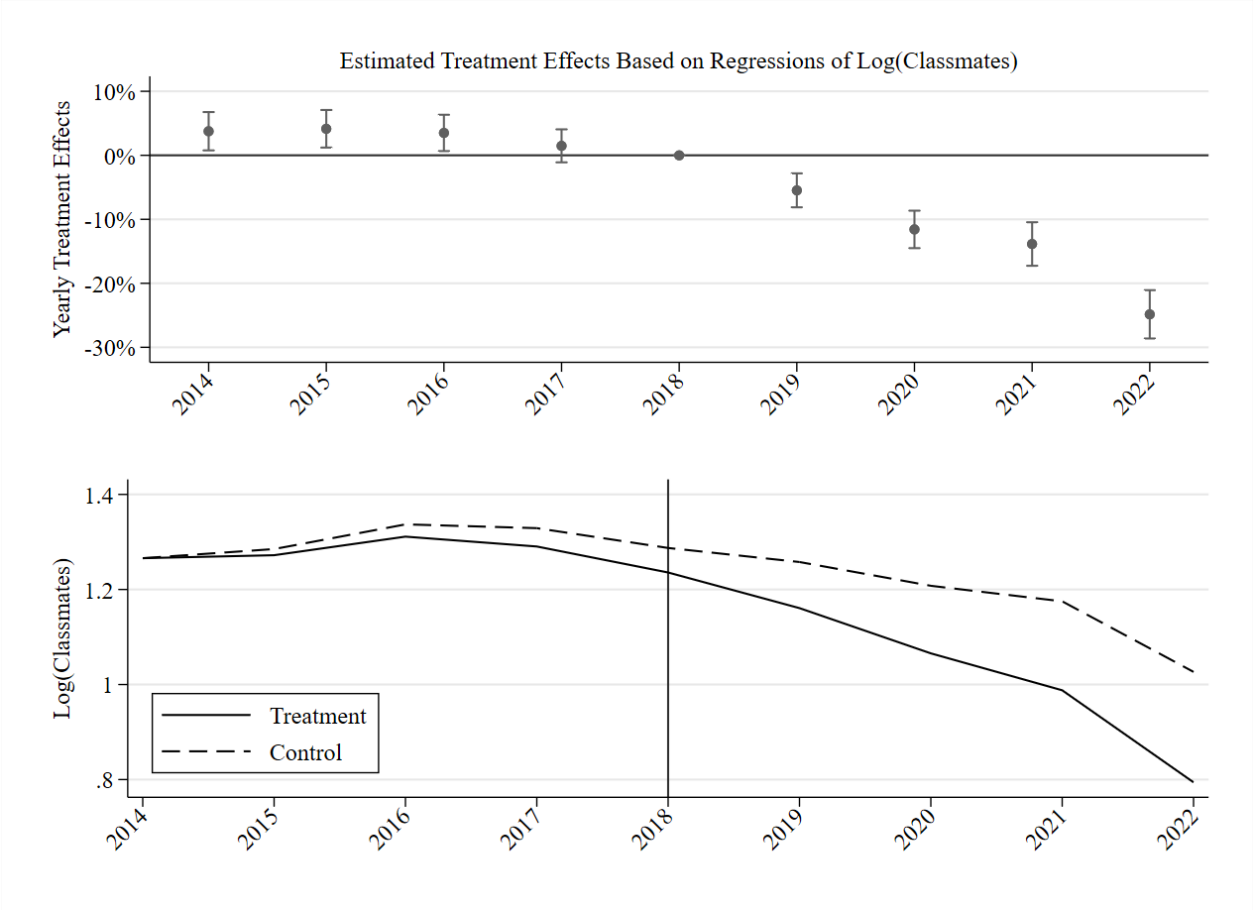


Figure 8. **Effect Dynamics: Classmates' Shift Away from Chip Manufacturing Jobs**

The first figure highlights time-varying effects of U.S. protectionism on the number of classmates of individuals skilled in chip manufacturing, landing science and engineering jobs. These estimates are based on a difference in differences approach according to specification (12), which accounts for fixed effects across country × job category × degree, country × year, and degree × year. Each point estimate is provided alongside a 95% confidence interval. The second figure illustrates trend comparisons between the treated group (classmates who find engineering and science jobs) and the control group (classmates entering jobs in administration, finance, marketing, operations, and sales). In these trend analyses, data adjustments are made to exclude the influences of fixed effects for country × job category × degree, country × year, and degree × year. Details on the data collection methodology and the definitions of variables employed can be found in Sections B.1.4 and B.2, respectively.



Internet Appendix for

When Protectionism Kills Talent

A Proof of Propositions

Proposition 1

Take the first-order conditions of the representative household's utility w.r.t the domestic and foreign chip goods, we have:

$$Y^{\frac{1}{\eta}}\alpha_C^{\frac{1}{\eta}}Y_C^{-\frac{1}{\eta}} = \lambda P_C \Rightarrow Y_C = (\lambda P_C)^{-\eta}\alpha_C Y \tag{A.1}$$

$$Y^{\frac{1}{\eta}}\alpha_O^{\frac{1}{\eta}}Y_O^{-\frac{1}{\eta}} = \lambda P_O \Rightarrow Y_O = (\lambda P_O)^{-\eta}\alpha_O Y, \tag{A.2}$$

where $Y \equiv \left(\alpha_C^{\frac{1}{\eta}}Y_C^{\frac{\eta-1}{\eta}} + \alpha_O^{\frac{1}{\eta}}Y_O^{\frac{\eta-1}{\eta}}\right)^{\frac{\eta}{\eta-1}}$, and λ is the Lagrange multiplier associated with the household's budget constraint. Substitute Equations (A.1) and (A.2) into the household budget constraint (Equation 2), we have:

$$\begin{aligned} I &= P_O(\lambda P_O)^{-\eta}\alpha_O Y + P_C(\lambda P_C)^{-\eta}\alpha_C Y \\ &= \lambda^{-\eta}\left[P_O(1-\eta)\alpha_O + P_C(1-\eta)\alpha_C\right]Y \\ &= \lambda^{-\eta}P^{1-\eta}Y, \end{aligned} \tag{A.3}$$

where $P = \left[P_O^{1-\eta}\alpha_O + P_C^{1-\eta}\alpha_C\right]^{\frac{1}{1-\eta}}$ is the composite price index. Substitue Equation (A.3) into Equation (A.1), we get:

$$Y_C = I(P^{1-\eta}Y)^{-1}P_C^{-\eta}\alpha_C Y = \alpha_C I P^{\eta-1}P_C^{-\eta}. \tag{A.4}$$

Use the firm's first-order conditions in Equation (5), we can express firm j's labor demand as:

$$d + f = \left[\frac{W}{z\theta(P_C - v)}\right]^{\frac{1}{\theta-1}}. \tag{A.5}$$

We have J symmetric firms in the economy, equating their total labor demand to the labor supply of foreign and domestic workers, we have the labor market clearing condition in Equation (7). Give firms' optimal labor demand, we can express the total output of domestic chip products in the economy as:

$$Y_C = Jy = Jz(d_j + f_j)^\theta = Jz\left[\frac{W}{z\theta(P_C - v)}\right]^{\frac{\theta}{\theta-1}}, \tag{A.6}$$

which we substitute into Equation (A.4) to obtain the product market clearing condition in Equation (8), which we reproduce below:

$$Jz\left[\frac{W}{z\theta(P_C - v)}\right]^{\frac{\theta}{\theta-1}} = \alpha_C I P^{\eta-1} P_C^{-\eta}, \tag{A.7}$$

which we can rewrite into:

$$Jz^{\frac{1}{1-\theta}}\left(\frac{W}{\theta}\right)^{\frac{\theta}{\theta-1}} = \alpha_C I(P_C - v)^{\frac{\theta}{\theta-1}} P^{\eta-1} P_C^{-\eta} = \alpha_C I(P_C - v)^{\frac{\theta}{\theta-1}} P_C^{-1}\left(\frac{P}{P_C}\right)^{\eta-1}. \tag{A.8}$$

We can verify that the RHS of Equation (A.8) is strictly decreasing in P_C for all $\theta \in (0, 1)$ and $\eta \geq 1$. Therefore, Equation (A.8) implies that the equilibrium wage rate W is a strictly increasing function of the domestic output price, P_C, and similarly, we can show that W is strictly increasing in z, and strictly decreasing in v. We can also verify these relationships

using the implicit function theorem by calculating:

$$\frac{\partial W}{\partial P_C} = \frac{1-\theta}{\theta}\eta\frac{W}{P_C} + \frac{W}{P_C - v} + \frac{W(\theta-1)}{\theta}(1-\eta)\alpha_C P^{\eta-1}P_C^{-\eta} > 0 \tag{A.9}$$

$$\frac{\partial W}{\partial z} = \frac{W}{\theta z} > 0 \tag{A.10}$$

$$\frac{\partial W}{\partial v} = \frac{-W}{P_C - v} < 0. \tag{A.11}$$

Thus, we can write $W = w(P_C, z, v)$, with $\frac{\partial w(P_C,z,v)}{\partial P_C} > 0$, $\frac{\partial w(P_C,z,v)}{\partial z} > 0$, and $\frac{\partial w(P_C,z,v)}{\partial v} < 0$. In the subsequent analysis, we use w to denote the implicit function $W = w(P_C, z, v)$. We plug this relationship into the labor market clearing condition (Equation 7) to obtain:

$$\begin{aligned} J\left(\frac{\alpha_C I P^{\eta-1}P_C^{-\eta}}{Jz}\right)^{\frac{1}{\theta}} &= S_D\left[w(P_C,z,v)\right] + \lambda S_F\left[w(P_C,z,v)\right] \\ \Leftrightarrow Az^{\frac{-1}{\theta}}P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}} &= S_D\left[w(P_C,z,v)\right] + \lambda S_F\left[w(P_C,z,v)\right], \end{aligned} \tag{A.12}$$

where $A \equiv J(\frac{\alpha_C I}{J})^{\frac{1}{\theta}}$ is a constant. The LHS of Equation (A.12) is strictly decreasing in P_C, and the RHS is strictly increasing in P_C, implying a unique product price and wage rate.

Proposition 2

We define the following based on Equation (A.12)

$$\Gamma \equiv Az^{\frac{-1}{\theta}}P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}} - S_D\left[w(P_C,z,v)\right] - \lambda S_F\left[w(P_C,z,v)\right] = 0. \tag{A.13}$$

Take first order condition of Γ w.r.t the equilibrium product price, and protectionist policies, as represented by z, λ, and v, we have:

$$\frac{\partial \Gamma}{\partial P_C} = Az^{-\frac{1}{\theta}}\frac{\partial\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} - \left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\frac{\partial w}{\partial P_C} < 0 \tag{A.14}$$

$$\frac{\partial \Gamma}{\partial z} = -\frac{1}{\theta} z^{-\frac{1}{\theta}-1} A \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C} \right)^{\frac{\eta-1}{\theta}} \right] - \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{\partial w}{\partial z} < 0 \tag{A.15}$$

$$\frac{\partial \Gamma}{\partial \lambda} = -S_F < 0 \tag{A.16}$$

$$\frac{\partial \Gamma}{\partial v} = -\left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{\partial w}{\partial v} > 0. \tag{A.17}$$

From the above equations, we can conclude that $\frac{\partial P_C}{\partial z} = -\left(\frac{\partial \Gamma}{\partial z}\right)\left(\frac{\partial \Gamma}{\partial P_C}\right)^{-1} < 0$. Simiarly, we can show that $\frac{\partial P_C}{\partial \lambda} < 0$, and $\frac{\partial P_C}{\partial v} > 0$. Plugging this result back into the consumer's optimal demand Equation (A.1). We can conclude that the higher subsidy increases firms' equilibrium production, while tighter H-1B restrictions (smaller λ) and higher tariffs on raw materials (larger v) lowers equilibrium output.

Proposition 3

we calculate the employment effect of greater subsidy, z, as the following:

$$\begin{aligned}
\frac{\partial \left(S_D + \lambda S_F \right)}{\partial z} &= \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \times \left(\frac{\partial w}{\partial z} + \frac{\partial w}{\partial P_C} \times \frac{\partial P_C}{\partial z} \right) \\
&= \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \times \left\{ \frac{\partial w}{\partial z} + \frac{\partial w}{\partial P_C} \times \left[-\left(\frac{\partial \Gamma}{\partial z} \right) \times \left(\frac{\partial \Gamma}{\partial P_C} \right)^{-1} \right] \right\} \\
&= \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \times \\
&\quad \left\{ \frac{w}{\theta z} + \frac{\partial w}{\partial P_C} \frac{\frac{1}{\theta} z^{-\frac{1}{\theta}-1} A P_C^{-\frac{1}{\theta}} \left(\frac{P}{P_C} \right)^{\frac{\eta-1}{\theta}} + \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{w}{\theta z}}{z^{-\frac{1}{\theta}} A \frac{\partial \left[P_C^{\frac{-1}{\theta}} \left(\frac{P}{P_C} \right)^{\frac{\eta-1}{\theta}} \right]}{\partial P_C} - \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \times \frac{\partial w}{\partial P_C}} \right\}
\end{aligned} \tag{A.18}$$

$$\begin{aligned}
&= \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{w}{z\theta} \times \left\{ 1 + \frac{B + \frac{\partial w}{\partial P_C} \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right)}{-C - \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{\partial w}{\partial P_C}} \right\} \\
&= \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{w}{z\theta} \times \left\{ \frac{C - B}{C + \left(\frac{\partial S_D}{\partial w} + \lambda \frac{\partial S_F}{\partial w} \right) \frac{\partial w}{\partial P_C}} \right\},
\end{aligned} \tag{A.19}$$

where we define:

$$B \equiv \frac{\partial w}{\partial P_C}\frac{1}{\theta}z^{-\frac{1}{\theta}-1}\frac{\theta z}{w}A\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right] > 0$$
$$C \equiv -z^{-\frac{1}{\theta}}A\frac{\partial\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} > 0.$$

Using Equation (A.9), we can verify that $B < C$. we also know that $\frac{\partial w}{\partial P_C} > 0$, which implies that $\frac{\partial(S_D+\lambda S_F)}{\partial z}$ is strictly increasing in $\left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)$, meaning that either more restrictive H-1B policy (smaller λ) or less elastic labor supplies (smaller $\frac{\partial S_D}{\partial w}$ or $\frac{\partial S_F}{\partial w}$ would diminish the effect of stimulative subsidies.

Proposition 4

Finally, we examine the employment effect of more restrictive labor market protectionist policies:

$$\begin{aligned}
\frac{\partial\left(S_D+\lambda S_F\right)}{\partial\lambda} &= S_F + \left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\times\left(\frac{\partial w}{\partial P_C}\right)\times\left(\frac{\partial P_C}{\partial\lambda}\right) \\
&= S_F + \left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\times\left(\frac{\partial w}{\partial P_C}\right)\times\left[-\left(\frac{\partial\Gamma}{\partial\lambda}\right)\times\left(\frac{\partial\Gamma}{\partial P_C}\right)^{-1}\right] \\
&= S_F + \left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\times\left(\frac{\partial w}{\partial P_C}\right)\times\frac{S_F}{z^{-\frac{1}{\theta}}A\frac{\partial\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} - \left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\frac{\partial w}{\partial P_C}} \\
&= S_F + \frac{S_F}{z^{-\frac{1}{\theta}}A\frac{\partial\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C}\left[\left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\frac{\partial w}{\partial P_C}\right]^{-1} - 1} = S_F + \frac{S_F}{D},
\end{aligned} \tag{A.20}$$

where we define:

$$D \equiv z^{-\frac{1}{\theta}}A\frac{\partial\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C}\left[\left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)\frac{\partial w}{\partial P_C}\right]^{-1} - 1 < -1. \tag{A.21}$$

Therefore, Equation (A.20) implies that the $\frac{\partial(S_D+\lambda S_F)}{\partial\lambda}$ is strictly increasing in the size of foreign workforce, $S_F(w)$.

In addition, because $A > 0$ and $\frac{\partial\left[P_C^{\frac{-1}{\theta}}\left(\frac{P}{P_C}\right)^{\frac{\eta-1}{\theta}}\right]}{\partial P_C} < 0$. Therefore, $\frac{\partial(S_D+\lambda S_F)}{\partial\lambda}$ is also strictly decreasing in $\left(\frac{\partial S_D}{\partial w} + \lambda\frac{\partial S_F}{\partial w}\right)$, meaning that either more restrictive H-1B policy (smaller λ) or less elastic labor supplies (smaller $\frac{\partial S_D}{\partial w}$ or $\frac{\partial S_F}{\partial w}$) would amplify the adverse effect of the H-1B restriction on hiring.

B Data Description

In this section, we outline the methodology behind our data collection process (see Section B.1) and provide detailed descriptions of the variables used in our study (see Section B.2).

B.1 Methodology for Constructing Dataframes from Revelio Labs and Additional Descriptive Statistics

The dataset utilized in our study is sourced from Revelio Labs, which specializes in providing granular, individual-level employment data.[29] This dataset encompasses extensive user-specific details, including current and past employment positions, educational backgrounds, names, skill sets, and demographic information, with a temporal benchmark of March 2023. We construct three principal dataframes for analysis: (i) the active labor force possessing chip manufacturing skills, (ii) the dynamics within the labor force of chip manufacturers, and (iii) annual cohorts of students who share educational affiliations with individuals skilled in chip manufacturing. Sections B.1.1,B.1.3, and B.1.4 below describe the methodology employed to develop these dataframes, respectively. We also provide detailed descriptive statistics in each section to augment the discussion in the main text.

[29] A detailed description of dataframes can be found on Revelio website: https://www.data-dictionary.reveliolabs.com/.

B.1.1 The Active Labor Force Possessing Chip Manufacturing Skills

The process begins with identifying individuals with semiconductor skills within the Revelio dataset. This is achieved by filtering the skill_file dataset to include only those entries where the 'skill_k75' variable—Revelio's proprietary method for clustering skills reported by individuals or their connections—equals "electronics / semiconductors / design of experiments." This category encompasses a broad spectrum of skills related to the semiconductor field, including electronics, circuit design, semiconductor fabrication, and integrated circuit design, among others. Specifically, these skills are: *logic design, circuit design, pcb design, soc, semiconductors, verilog, ic, asic, digital electronics, vhdl, doe (design of experiments), metrology, failure analysis, power supplies, semiconductor industry, integrated circuits (ic), thin films, silicon, analog, electro-mechanical, hardware development, embedded c, fpga, cadence, vlsi, ni multisim, microcontrollers, power electronics, connectors, tcl, xilinx, digital signal processors, proteus, rtl coding, xilinx ise, orcad, field-programmable gate arrays (fpga), rtl design, altera, product engineering, mplab, pspice, autosar, pcie, schematic capture, mixed signal, analog circuit design, signal integrity, x86, synopsys tools, semiconductor fabrication, cadence virtuoso, intel, photolithography, mems, ncsim, modelsim, electronics, formal verification, systemverilog, integrated circuit design, functional verification, hardware architecture, multisim, microelectronics, microprocessors, microchip pic, vacuum, electronic engineering, computer architecture, processors, electrical machines, 8051 microcontroller, pcb layout design, application-specific integrated circuits (asic), system on a chip (soc), circuit analysis, keil, logic synthesis, cst microwave studio, hardware design, agilent ads, pll, cmos, power management, hfss, eda, embedded software programming, sputtering, semiconductor process, electronics hardware design, physical verification, can, tcl-tk, fpga prototyping, pvd, process integration, cvd, plasma etch, pecvd, computer engineering, spice, orcad capture cis, physical design, low-power design, arm cortex-m, very-large-scale integration, canoe, static timing analysis, dft, dsp, drc, semiconductor device, device characterization, cadence spectre, analog circuits, timing closure, ltspice, can bus, digital circuit design, very-large-scale integration*

(vlsi), electronic circuit design, yield, uvm, field-programmable gate arrays, system verilog, inverters, serdes, compilers, gage r&r, primetime, systemc, embedded c++, flash memory, semiconductor manufacturing, integrated circuits, application-specific integrated circuits, system on a chip.

Given the repetition in a few skill labels, such as 'integrated circuits' appearing in various forms, we later consolidate similar skills into unified categories for clarity. Utilizing this refined data, we construct a dataframe centered around Revelio's unique individual identifiers. This dataframe includes dummy variables for each skill, indicating whether an individual possesses that particular skill. For instance, if an individual has listed only 'orcad capture cis' as their skill, then all dummy variables except for 'orcad capture cis' will be set to zero, while the dummy for 'orcad capture cis' will be marked as one. This methodical approach enables us to systematically categorize and analyze the semiconductor skills present within the dataset.

We then merge the above dataframe with position_file, which contains the individual level position data, and company_ref, which contains static firm data. We remove rows lacking 'naics_code' data (0.09% of the firms), which are essential for mapping into two- and six-digit NAICS codes. The resulting dataset comprises records of job positions held by individuals identified by their chip manufacturing skills, indicated through dummy variables. To isolate active employees within this dataset, we apply filters to select only those whose positions were active as of March 1, 2023, and whose records include a valid name for the ultimate parent company. Additionally, we exclude records where the country field is marked as 'empty'.

In this refined dataset, we determine the distinct number of individuals according to country, firm, and industry. When conducting analyses at the firm level, which involve categorizing employees based on their seniority, we adopt two key strategies: positions missing seniority information are omitted, and we set guidelines for handling cases where an individual holds more than one position simultaneously. For instance, should an individual be

documented as having concurrent employment (such as an academic with a role at Penn State University and another at Intel within the same period), we exclusively retain the position that ranks higher in seniority. This method ensures the accuracy of our data by eliminating the potential for missing data and double-counting individuals.

In the context of employment within U.S. government entities, our analysis identifies significant numbers of individuals working for various departments and agencies, showcasing the breadth of employment within this sector. Notable employers include the United States Navy, US Air Force, The United States Army, Sandia National Laboratories, Jet Propulsion Laboratory, Federal Aviation Administration, US Department of Defense, Lawrence Livermore National Laboratory, National Aeronautics & Space Administration, and the United States Marine Corps.

B.1.2 Active Semiconductor Workforce Descriptive Statistics – Continues

In this section, we discuss the characteristics of the active semiconductor workforce around the world, to augment the discussion dedicated in Section **??** to mainly the workforce in the U.S. to save space. Table 1 provides the distribution of the physical location of 1.6 million active employees with chip manufacturing skills as of March 2023 across the world. United States is at the top of the list of countries hosting these skills, with 680,602 employees being physically in the US., with a large fraction (480,193) of these employees work as an engineer, while 49,515 are scientists. India has 165,352 employees with chip skills and a larger fraction of these people (almost 130,000) are engineers. Their job as of March 2023 is their 4^{th} job on average, and the average seniority is similarly at around 3, –i.e., at the associate level. The average salary is much lower though, at \$12,751.[30] Table 1 also highlights the employment and economic characteristics across prominent European countries. For instance, the United Kingdom ranks third with a total of 88,527 employees, heavily skewed towards engineering roles with 57,927 engineers, and an average salary of \$58,110.89. Germany follows, with

[30]India has a 2022 PPP conversion factor of 22.88. See, e.g., https://data.worldbank.org/indicator/PA.NUS.PPP.

43,597 total employees, 28,759 of whom are engineers, boasting a higher average salary of $79,377.39. France and Italy also show significant figures, with total employments of 38,024 and 30,545, respectively, and engineers forming the largest job category in each country. Canada ranks fourth, surpassing all European countries in the number of active employees, 63,376 in total, except for the UK.[31]

Table 1 further illustrates that countries such as India, Brazil, Pakistan, Turkey, and Malaysia have a significant number of engineers with chip manufacturing skills and experience, as indicated by their job positions and tenure lengths. However, these engineers are compensated at a lower rate compared to their counterparts in other countries. For China, the data indicates a total employment of 28,664 individuals with chip manufacturing skills. Among these, engineers represent the largest job category with 16,330 jobs, highlighting China's substantial focus on engineering talent within the industry. The average tenure for these positions in China is reported at 3,330.75 days, suggesting a relatively experienced workforce. Despite this expertise, the average salary is $28,236.07, which also is lower compared to Western countries. Figure 1 further illustrates the global distribution of employees with chip manufacturing skills who are actively employed as of March 2023, including countries not shown in Table 1.

B.1.3 Labor Force Dynamics of U.S. Chip Manufacturers

In our study, we delineate chip manufacturing firms using specific NAICS codes as the basis for classification. The initial step in our methodology involves processing the data from the company_ref dataframe, which entails iterating through rows to eliminate those lacking NAICS codes. Out of the 19,448,263 rows processed, 1,361,625 are retained, corresponding to firms identified by their NAICS codes, while 18,086,638 rows are discarded. The firms preserved in this filtered dataset are those associated with NAICS codes [334413, 334515, 334418, 333242, 333295, 333248, 333994], which are relevant to the chip manufacturing

[31] As of 2022, United Kingdom, Germany, France, Italy, China and Canada have (World Bank) PPP conversion factors of 0.68, 0.73, 0.70, 0.63, 3.99, and 1.23, respectively.

industry. Revelio's sample contains the following NAICS codes: 333242, 333994, 334413, 334418, and 334515.

Subsequent to this filtration, we integrate this refined list of firms with data from the position_file, which contains detailed information on individual employment positions. This integration aims to construct a person-firm-year panel, enabling a longitudinal study of employment patterns. To refine this panel further, we implement the following filters: we exclude records with undefined start dates (i.e., labeled as '\\N'), ensure that the start date precedes the end date, remove entries where the country field is 'empty'.

The transformation process then involves expanding each row of the dataframe to account for each year an individual held a position, thus adding a temporal dimension to the dataset. Consider for example a record which details the employment of an individual assigned user ID 301252435 and position ID 6893505588650110490 at "hohenloher spezialmöbelwerk schaffitzel gmbh" (identified by Revelio company ID 872817 and FactSet entity ID 08QGZ3-E), a German-based company. The tenure extended from February 1, 2016, to March 1, 2023. In this period, the individual served as the "Assistent der Geschäftsleitung" (Assistant to the Executive Management), a role within the accounting and finance job category of the finance sector. Characterized by an entry-level seniority (seniority level 1), this position came with an annual salary of €37,108.413. The data concerning this employment will be expanded into panel data covering the years 2016 to 2023.

We emphasize the use of yearly panels over monthly panels to mitigate the introduction of noise from inaccurately reported start dates on professional platforms like LinkedIn. This approach addresses the issue of 'false' turnover observed at the start and end of years, a common artifact when individuals do not specify the exact month of employment commencement or termination. Our methodological choice is validated by the close alignment of our yearly employment counts with those reported by LinkedIn, indicating the reliability of our data aggregation technique.

The final step in our analysis involves aggregating the unique number of individuals

employed at each firm within a given year across different categories, thereby providing a comprehensive overview of employment trends in the chip manufacturing sector based on a person-firm-year panel. This aggregate data serves as the foundation for our empirical analysis, offering insights into the dynamics of the labor market within this industry.

After transforming individual data into a person-firm-year panel format, we proceed to calculate the number of employees at each U.S. manufacturing firm by job category (such as Admin, Engineer, Finance, Marketing, Operations, Sales, and Scientist) for each year, creating a detailed firm-job category-year dataset. From 2014 onwards, this dataset encompasses 5,436 distinct firms. To refine our analysis and exclude very small (micro) firms, and to ensure reliable counterfactual units (i.e., alternative job categories), we apply the following criteria: only firms that have been operational for at least three years by 2014, determined by the earliest LinkedIn profiles of their employees, are included. Additionally, we only consider firm-years that feature at least five job categories. This approach ensures the availability of at least three alternative job categories for scenarios where engineering and scientific positions are considered treated. Following these restrictions, the dataset is narrowed down to 1,153 unique firms, resulting in 68,949 data points. To further enhance data quality, we apply winsorization to all firm-job category-year variables at the 2.5% level to eliminate outliers.

In the dataset related to firm-country-job category-year (referenced in Table 8 and described in Panel B of Table 4), we apply additional criteria to exclude 'phantom' segment countries. These criteria involve removing countries that have data for fewer than 50 unique firms over the sampling period. Additionally, we exclude any firm-country-year group that contains fewer than two observations. This is to ensure that within a given year and country, firms are represented in at least two job categories.

B.1.4 Annual Cohorts of Students Who Share Educational Affiliations With Individuals Skilled in Chip Manufacturing

We also construct a dataset focusing on the classmates of individuals possessing chip manufacturing skills, drawing on various data sources provided by Revelio. This dataset is formulated by initially creating a dataframe of individuals with chip manufacturing expertise, as detailed in Section B.1.1, with the notable distinction that our selection does not limit itself to individuals currently employed. We begin by filtering for the latest educational degrees of these individuals using the education_file. With this filtered data, we further analyze the education_file to pinpoint individuals who graduated from the same school and program in the same year. During this process, we apply stringent filters to ensure data quality, excluding rows where details such as 'school', 'enddate', 'field_raw', and 'degree' are either not provided, marked as "\N", or labeled as "empty". After these exclusions, we only keep those rows with valid 'enddate's.

To identify a person's classmates accurately, we apply criteria ensuring they share the same 'school', 'degree', and 'field_raw', and have graduated in the same year. This methodological approach allows us to comprehensively map out the educational networks surrounding individuals skilled in semiconductor manufacturing. Subsequently, we explore the position_file, which contains data on the jobs the classmates take after their graduation. We impose certain restrictions on the initial positions these classmates take after graduating from the same programs as the people with chip manufacturing skills. This includes keeping jobs that are acquired only after graduation date, focusing on positions obtained within two years of graduating, prioritizing the first job started if multiple jobs are taken simultaneously, and excluding jobs without specified 'country' data. We also drop classmates from high schools and associate degree programs. Through these filters, we compile data reflecting the employment characteristics of the classmates of individuals with chip manufacturing skills. Importantly, to prevent double-counting, we count the number of unique ID numbers associated with individuals, thereby avoiding the duplication of counts for classmates

possessing chip manufacturing skills within a specific year.

B.1.5 Additional Tests on Annual Cohorts of Chip Manufacturing Education Using Data From The Department of Education

In the main text, we utilize Revelio data to examine cohorts of students that enter chip manufacturing careers along with their classmates. In this section, we revisit this question using data from the U.S. Department of Education on degree completions in the U.S. In particular, we use the Integrated Postsecondary Education Data System (IPEDS), which is part of the National Center for Education Statistics (NCES). This data is not self reported and therefore less likely to be prone to measurement issues, and it allows us to double-check our earlier findings with a second dataset.

NCES data is publicly available at https://nces.ed.gov/ipeds/datacenter/ under 'Complete Data Files' and 'Completions'. These files contain detailed information on the number of graduates from each institution in the U.S. (identified with unique UNITID identifiers) across different degrees (denoted with unique 6-digit CIPCODE identifiers) and degree levels (AWLEVEL). The number of graduates is measured in aggregate (CTOTALT) and based on visa status (CNRALT), which measures the number of Non-U.S. graduates, referring to students who are not citizens or nationals of the United States, i.e., in the country on a visa or temporary basis without the right to remain indefinitely.

We focus on students' initial major completions and identify degree programs (CIP codes) related to chip manufacturing by analyzing the NCES CIP code descriptions, which explain how each degree prepares students for specific careers.[32] These files define each degree type in the U.S. (consistently across institutions) and describe the career preparation each degree offers. For example, CIP code '15.0616' refers to '*Semiconductor Manufacturing Technology/Technician*' and is described as a 'program that prepares individuals to apply basic engineering principles and technical skills to operate and monitor equipment for the fabrica-

[32]These descriptions are publicly available here: https://nces.ed.gov/ipeds/cipcode/resources.aspx?y=56. See, e.g., the CIP Codes 2020 spreadsheet.

tion of semiconductors or microchips from silicon wafers, and to troubleshoot, maintain, and repair the specialized equipment used in this process. Includes instruction in AC and DC circuits, digital fundamentals, solid state devices, manufacturing processes, vacuum principles and technology, industrial electronics, quality assurance, and semiconductor manufacturing technology.'

Using NCES degree descriptions, we identify U.S. engineering and technician degrees where the CIP family (the first two digits of the CIP code) is 14, 15, 46, 47, or 48. We then determine which of these degrees are related to chip manufacturing by searching program titles, CIP definitions, and examples for keywords `chip|semicond|circuit|wafer|silicon|microelec|fabless|microchip|MEMS|lithograph|etching|microfab|photonic|manufact` in regular expressions.

In doing so, we identify the following chip manufacturing-related engineering and technician degrees (with their corresponding CIP codes).[33] We categorize these degrees in Bachelor & Pre-Bachelor categories (i.e., 1<AWLEVEL<=5) and Graduate categories (i.e., AWLEVEL==7 or AWLEVEL==7):

- 140103: Applied Engineering
- 140902: Computer Hardware Engineering
- 141801: Materials Engineering
- 141901: Mechanical Engineering
- 143601: Manufacturing Engineering
- 144701: Electrical and Computer Engineering
- 150001: Applied Engineering Technologies/Technicians
- 150303: Electrical, Electronic, and Communications Engineering Technology/Technician
- 150306: Integrated Circuit Design Technology/Technician
- 150403: Electromechanical/Electromechanical Engineering Technology/Technician
- 150613: Manufacturing Engineering Technology/Technician

[33]The following CIP codes and titles were identified as false positives and excluded from the treatment group: 141004 (Telecommunications Engineering), 142001 (Metallurgical Engineering), 142801 (Textile Sciences and Engineering), 144001 (Paper Science and Engineering), 144101 (Electromechanical Engineering), 144501 (Biological/Biosystems Engineering), 144802 (Power Plant Engineering), 150607 (Plastics and Polymer Engineering Technology/Technician), 150611 (Metallurgical Technology/Technician), 150801 (Aeronautical/Aerospace Engineering Technology/Technician), 150803 (Automotive Engineering Technology/Technician), and 150806 (Marine Engineering Technology/Technician).

- 150616: Semiconductor Manufacturing Technology/Technician
- 150617: Composite Materials Technology/Technician
- 150702: Quality Control Technology/Technician
- 150805: Mechanical/Mechanical Engineering Technology/Technician
- 151201: Computer Engineering Technology/Technician
- 151203: Computer Hardware Technology/Technician
- 151305: Electrical/Electronics Drafting and Electrical/Electronics CAD/CADD
- 151306: Mechanical Drafting and Mechanical Drafting CAD/CADD
- 151307: 3-D Modeling and Design Technology/Technician
- 151501: Engineering/Industrial Management
- 470101: Electrical/Electronics Equipment Installation and Repair Technology/Technician, General
- 470105: Industrial Electronics Technology/Technician
- 470302: Heavy Equipment Maintenance Technology/Technician
- 480501: Machine Tool Technology/Machinist
- 480503: Machine Shop Technology/Assistant
- 480511: Metal Fabricator

The strategy above provides a sample of students that closely matches our Revelio data in terms of relevant programs and student numbers. For instance, Revelio data includes an undergraduate cohort of 65,290 students in chip manufacturing-related education, while IPEDS data, as of 2017, lists 60,990 students in similar programs. We classify chip manufacturing-related degrees as treated units and all other degrees as control units, comparing both groups before and after the onset of the protectionist era in 2018. We employ the below difference-in-differences specification:

$$y_{d,t} = \tau \text{Treated}_d \times \text{Post}_t + \gamma_d + \theta_t + \epsilon_{d,t}. \tag{B.22}$$

Our analysis focuses on $y_{d,t}$, which represents either Log(Completions$_{d,t}$) or Log(Non-U.S. Resident Completions$_{d,t}$). These denote, respectively, the number of all students graduating from degree d in the U.S. in year t, and the number of non-U.S. resident students graduating

from degree d in the U.S. in year t. Treated_d is set to one for the chip manufacturing-related engineering and technician degrees mentioned above, and zero otherwise. Post_t is one for years after 2018 and zero otherwise. Table B4 presents our findings.

[Table B4 about here]

As shown in Table B4, we identify a 14% decline in the number of graduates from bachelor and pre-bachelor degrees in the U.S. (Column 1) and a 15% decline in postgraduate degrees (Column 3). Furthermore, the reduction in the number of non-U.S. resident graduates is also significant, amounting to nearly 17% and 29% in undergraduate and postgraduate programs, as shown in Columns 2 and 4, respectively. Overall, these results align with our findings based on the Revelio data shown in Panel A of Table 10, collectively suggesting a reduction in the number of chip manufacturing students in the post-protectionist era.

B.2 Variable Definitions

This section provides detailed descriptions of the variables used in our study. The variables presented in Panel B of Table 4 correspond to those introduced in Panel A, yet they are analyzed at a more granular level, encompassing firm, country, job category, and year. For the sake of conciseness, their descriptions are not repeated here.

- **Log(Emp$_{i,j,t}$):** The natural logarithm of the sum of one and the total number of employees in job category j at company i in year t.
- **Log(Hiring$_{i,j,t}$):** The natural logarithm of the sum of one and the number of new hires in job category j at company i in year t. New hires are employees whose initial year of work at the firm begins is year t.
- **Log(Separation$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees in job category j leaving company i in year t. Leaving the company refers to the employees for whom year t marks the final year of their employment at the firm.

- **Log(Turnover$_{i,j,t}$):** The natural logarithm of the sum of one and the total of new hires and leaving employees in job category j at company i in year t.

- **Hiring Rate$_{i,j,t}$:** The ratio of the number of new hires in job category j at company i in year t to the total number of employees in the same job category at the company in the previous year $(t-1)$.

- **Separation Rate$_{i,j,t}$:** The ratio of the number of employees leaving in job category j at company i in year t to the total number of employees in the same job category at the company in the previous year $(t-1)$.

- **Net Hiring Rate$_{i,j,t}$:** The difference between the hiring rate and the separation rate for job category j at company i in year t.

- **Turnover Rate$_{i,j,t}$:** The sum of the hiring rate and the separation rate for job category j at company i in year t.

- **Log(FirstJobEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees in job category j at company i whose first year of employment is t and who are newly hired without prior work experience.

- **Log(ExprEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees in job category j at company i who are hired in year t with previous work experience.

- **Log(JunPosEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees hired in year t for junior positions (seniority levels 1 to 3) in job category j at company i.

- **Log(MidSenPosEmp$_{i,j,t}$):** The natural logarithm of the sum of one and the number of employees hired in year t for mid-senior positions (seniority levels 4 and 5) in job category j at company i.

- **Seniority:** Defined as an ordinal variable between 1 and 7: 1. Entry Level (e.g., Software Engineer Trainee); 2. Junior Level (e.g., Junior Software QA Engineer); 3. Associate Level (e.g., Lead Electrical Engineer); 4. Manager Level (e.g., Superintendent Engineer); 5. Director Level (e.g., VP Network Engineering); 6. Executive Level (e.g., Director of Engineering, Backend Systems); 7. Senior Executive Level (e.g.,CFO; CEO)

- **Log(Cohort Size$_{c,d,j,t}$)**: This is the logged number of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

- **Log(Avg. Salary$_{c,d,j,t}$)** : This is the average first-job salaries of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

- **Avg. Seniority$_{c,d,j,t}$** : This is the average first-job seniority levels of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

- **Log(Tenure$_{c,d,j,t}$)**: This is the average first-job tenures of classmates, who graduated alongside individuals with chip manufacturing skills, in country c in year t, holding a degree d, and have secured jobs within job category j.

C Additional Findings

In this section, we present supplementary results not included but mentioned in the main text. Appendix Table B1 shows the results of our placebo test, examining the impact of U.S. protectionist policies on employment in science and engineering roles within U.S. firms, specifically those classified under the NAICS code 423690. This sector includes businesses primarily focused on the merchant wholesale distribution of electronic parts and equipment.

Examples of firms in this category include wholesalers of blank CDs/DVDs (as opposed to manufacturers of wafers) and blank diskettes (as opposed to manufacturers of chips). Our findings indicate no significant effects of U.S. protectionism on the employment levels within these firms.

Appendix Figures B3, B4, and B5 present effect dynamics and evidence for the observable counterpart of the parallel trends assumption for all other dependent variables from Tables 5 and 6 that were not displayed in the main body of the text. Appendix Figures B7 and B8 provide evidence from subsample tests that emphasize a shift away from science and engineering roles globally and trends in the global workforce among U.S. chip manufacturers, involving fewer employees in the U.S. but more in alternative locations such as Canada and European countries such as the Netherlands.

Appendix Table B1. **Placebo Test: Other Electronic Parts and Equipment Merchant Wholesalers**

This table presents our findings from our placebo test on how protectionism has influenced science and engineering employment at U.S. chip manufacturing companies, based on firms with NAICS code of 423690 (i.e., merchant wholesale distributors of electronic parts and equipment; except for electrical apparatus and equipment, wiring supplies, and construction materials, electrical and electronic appliances, and television and radio sets). Utilizing the difference-in-differences approach outlined in Equation (9), we analyze the effects on employment metrics. Panel A shows the effect on employee count, hiring practices, separation, and turnover, while Panel B focuses on these metrics in rate form instead of absolute numbers. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by $\star\star\star$, $\star\star$, and $\star$, respectively.

Panel A: Analysis of Chip Manufacturing Workforce				
	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	0.00	-0.02	-0.01	-0.02
	(0.14)	(-1.15)	(-0.35)	(-0.87)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	22,311	22,311	22,311	22,311
R-squared	0.967	0.816	0.799	0.842
Panel B: Analyses of Employment Growth				
	$\text{Hiring Rate}_{i,j,t}$	$\text{Separation Rate}_{i,j,t}$	$\text{Net Hiring Rate}_{i,j,t}$	$\text{Turnover Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.01	-0.00	-0.01	-0.01
	(-0.89)	(-0.19)	(-0.81)	(-0.76)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	22,311	22,311	22,311	22,311
R-squared	0.394	0.367	0.344	0.414

Appendix Table B2. **Effect Heterogeneity: U.S. vs. Non-U.S. Workforce and the Role of H-1B Hiring (Intensive Margins)**

This table reports our estimates of the heterogeneous effect of U.S. protectionism on workforce dynamics in U.S. chip manufacturing firms, both domestically and internationally, as well as among firms that rely on foreign talent and those that do not. The results are based on Equation (11). $\text{Log(Petitions}_i\text{)}$ indicates whether firm i sponsored H1B petitions in fiscal year 2017 based on USCIS's H-1B Employer Data Hub. Additional variable definitions are provided in Table 8. The analysis spans the years 2014 to 2022, utilizing clustered standard errors by firm. Statistical significance at 1%, 5%, and 10% levels are indicated by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

	Panel A: Analyses of Chip Manufacturing Workforce (N=231,696)							
	$\text{Log(Emp}_{i,c,j,t}\text{)}$	$\text{Log(Hiring}_{i,c,j,t}\text{)}$	$\text{Log(Separation}_{i,c,j,t}\text{)}$	$\text{Log(Turnover}_{i,c,j,t}\text{)}$	$\text{Log(Emp}_{i,c,j,t}\text{)}$	$\text{Log(Hiring}_{i,c,j,t}\text{)}$	$\text{Log(Separation}_{i,c,j,t}\text{)}$	$\text{Log(Turnover}_{i,c,j,t}\text{)}$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Log(Petitions}_i\text{)}$	-0.01*	-0.03***	-0.02***	-0.02	-0.02*	-0.03***	-0.02***	-0.02
	(-1.72)	(-4.83)	(-2.89)	(-1.59)	(-1.72)	(-4.78)	(-2.89)	(-1.59)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.03***	-0.04***	-0.01	-0.04***	-0.03***	-0.04***	-0.01	-0.04**
	(-2.90)	(-3.95)	(-1.26)	(-2.78)	(-2.91)	(-3.71)	(-1.16)	(-2.55)
$\text{Treated}_j \times \text{Post}_t \times \text{Log(Petitions}_i\text{)}$	0.02***	0.02*	0.02***	0.03***	0.02***	0.02*	0.02***	0.03***
	(2.84)	(1.82)	(4.56)	(2.97)	(2.84)	(1.84)	(4.57)	(2.99)
$\text{Post}_t \times \text{US}_c \times \text{Log(Petitions}_i\text{)}$	-0.01	0.01	0.02**	0.02*	-0.01	0.01	0.02***	0.02*
	(-1.07)	(1.33)	(2.63)	(1.93)	(-1.03)	(1.36)	(2.65)	(1.96)
$\text{Treated}_j \times \text{Post}_t$	-0.00	-0.05***	-0.04***	-0.07***				
	(-0.13)	(-4.24)	(-3.62)	(-4.65)				
R-squared	0.948	0.781	0.760	0.807	0.948	0.781	0.760	0.807
	Panel B: Analyses of Employment Growth (N=231,696)							
	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$	$\text{Hiring Rate}_{i,c,j,t}$	$\text{Separation Rate}_{i,c,j,t}$	$\text{Net Hiring Rate}_{i,c,j,t}$	$\text{Turnover Rate}_{i,c,j,t}$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Log(Petitions}_i\text{)}$	-0.00	0.00	-0.01***	-0.00	-0.00	0.00	-0.01***	-0.00
	(-1.51)	(0.58)	(-3.17)	(-0.79)	(-1.50)	(0.57)	(-3.13)	(-0.80)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.01**	-0.01**	-0.01	-0.02**	-0.01**	-0.01**	-0.00	-0.01**
	(-2.43)	(-2.32)	(-1.54)	(-2.60)	(-2.23)	(-2.28)	(-1.33)	(-2.45)
$\text{Treated}_j \times \text{Post}_t \times \text{Log(Petitions}_i\text{)}$	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
	(0.76)	(0.85)	(0.82)	(0.87)	(0.79)	(0.86)	(0.85)	(0.90)
$\text{Post}_t \times \text{US}_c \times \text{Log(Petitions}_i\text{)}$	-0.00	0.00	-0.00	-0.00	-0.00	0.00	-0.00	-0.00
	(-0.69)	(0.95)	(-1.44)	(-0.04)	(-0.64)	(0.96)	(-1.38)	(-0.00)
$\text{Treated}_j \times \text{Post}_t$	-0.02***	-0.00*	-0.01***	-0.02***				
	(-4.06)	(-1.84)	(-3.03)	(-3.72)				
R-squared	0.329	0.281	0.211	0.349	0.329	0.281	0.212	0.350
	Panel C: Analyses of Chip Manufacturing Workforce by Career Progression (N=231,696)							
	$\text{Log(FirstEmp}_{i,c,j,t}\text{)}$	$\text{Log(ExprEmp}_{i,c,j,t}\text{)}$	$\text{Log(JunEmp}_{i,c,j,t}\text{)}$	$\text{Log(MidSenEmp}_{i,c,j,t}\text{)}$	$\text{Log(FirstEmp}_{i,c,j,t}\text{)}$	$\text{Log(ExprEmp}_{i,c,j,t}\text{)}$	$\text{Log(JunEmp}_{i,c,j,t}\text{)}$	$\text{Log(MidSenEmp}_{i,c,j,t}\text{)}$
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c \times \text{Log(Petitions}_i\text{)}$	-0.02***	-0.02*	-0.02**	-0.01**	-0.02***	-0.02*	-0.02**	-0.01**
	(-4.84)	(-1.80)	(-2.21)	(-2.45)	(-4.88)	(-1.80)	(-2.21)	(-2.45)
$\text{Treated}_j \times \text{Post}_t \times \text{US}_c$	-0.00	-0.03***	-0.02**	-0.01	-0.00	-0.03***	-0.02**	-0.01
	(-0.83)	(-2.79)	(-2.40)	(-1.08)	(-1.08)	(-2.80)	(-2.49)	(-1.09)
$\text{Treated}_j \times \text{Post}_t \times \text{Log(Petitions}_i\text{)}$	0.01*	0.02***	0.02**	0.02***	0.01*	0.02***	0.02**	0.02***
	(1.77)	(2.97)	(2.20)	(4.15)	(1.78)	(2.98)	(2.20)	(4.17)
$\text{Post}_t \times \text{US}_c \times \text{Log(Petitions}_i\text{)}$	0.00	-0.01	-0.01	0.01	0.00	-0.01	-0.01	0.01
	(0.32)	(-1.03)	(-0.93)	(0.93)	(0.34)	(-1.00)	(-0.91)	(0.96)
$\text{Treated}_j \times \text{Post}_t$	-0.01***	0.01	0.00	-0.00				
	(-2.76)	(0.68)	(0.15)	(-0.25)				
R-squared	0.961	0.940	0.943	0.939	0.961	0.940	0.943	0.939
	Panel D: Controls for Panels A, B, and C							
Firm × Country × Job Cat. FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Country × Year FE	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Job Category × Year FE	No	No	No	No	Yes	Yes	Yes	Yes

Appendix Table B3. **U.S. Job Postings for Scientists and Engineers**

This table presents our findings on the impact of economic protectionism on job postings in the U.S. We report findings from difference-in-difference regressions at the job category (j) and year (t) levels. The job posting data is sourced from LinkUp's database, spanning 2007 to 2022. In Panel A, the treated categories include scientist and engineering roles, while the control group comprises the remaining job categories. We exclude "Medical Representative" and "Geologist" from the treated categories to focus specifically on engineers and scientists. In Panel B, we further refine the treated group by excluding "Data Analyst," "IT Project Manager," "IT Specialist," "Software Engineer," and "Sustainability Specialist." The final treated job categories include "Engineer," "Production Operator," "QA Tester," "Quality Assurance," "Scientist," "Technical Architect," and "Technician." The analysis covers the period from 2014 to 2022, with standard errors clustered at the job category level. Statistical significance at the 1%, 5%, and 10% levels is denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

Panel A: Job Posts for Engineers and Scientists			
	$\text{Log}(\text{JobPostCreation}_{j,t})$	$\text{Log}(\text{JobPostDeletion}_{j,t})$	$\text{Log}(\text{ActiveJobPosts}_{j,t})$
	(1)	(2)	(3)
$\text{Treated}_j \times \text{Post}_t$	0.11**	0.11**	0.13***
	(2.40)	(2.49)	(2.82)
Job Category FE	Yes	Yes	Yes
Year FE	Yes	Yes	Yes
Observations	432	432	432
R-squared	0.981	0.981	0.983
Panel B: Findings After Excluding Job Posts for Software Engineers, IT, and Data Science			
	$\text{Log}(\text{JobPostCreation}_{j,t})$	$\text{Log}(\text{JobPostDeletion}_{j,t})$	$\text{Log}(\text{ActiveJobPosts}_{j,t})$
	(1)	(2)	(3)
$\text{Treated}_j \times \text{Post}_t$	0.12**	0.12***	0.13***
	(2.69)	(2.70)	(3.18)
Job Category FE	Yes	Yes	Yes
Year FE	Yes	Yes	Yes
Observations	387	387	387
R-squared	0.981	0.981	0.983

Appendix Table B4. **Protectionism and U.S. Chip Manufacturing Degree Completions: Evidence from IPEDS Data by Residency Status**

This table shows estimates of the influence of protectionism on chip manufacturing degrees obtained in the U.S. The data is sourced from the U.S. Department of Education's Integrated Postsecondary Education Data System (IPEDS), focusing on degree completions in the U.S. for all students and for non-U.S. residents. Treated degree categories include U.S. engineering and technician degrees where the CIP family (the first two digits of the CIP code) is 14, 15, 46, 47, or 48. We determine which of these degrees relate to chip manufacturing by searching program titles, CIP definitions, and descriptions for keywords `chip|semicond|circuit|wafer|silicon|microelec|fabless|microchip|MEMS|lithograph|etching|microfab|photonic|manufact` using regular expressions. Control degrees include all other degrees. We analyze Log(Completions$_{d,t}$) and Log(Non-U.S. Resident Completions$_{d,t}$), representing the number of all students graduating from degree d in the U.S. in year t, and the number of non-U.S. resident students graduating from degree d in the U.S. in year t, respectively. Treated$_d$ is set to one for the chip manufacturing-related engineering and technician degrees mentioned above and zero otherwise, while Post$_t$ is one for years after 2018 and zero otherwise. Clustering is done at the CIP degree family level. See Section B.1.5 for additional variable descriptions and methodology. Statistical significance at the 1%, 5%, and 10% levels are denoted by $\star\star\star$, $\star\star$, and $\star$, respectively.

	Panel A: Bachelor & Pre-Bachelor Degrees		Panel B: Graduate Degrees	
	Log(Completions$_{d,t}$)	Log(Non-U.S. Resident Completions$_{d,t}$)	Log(Completions$_{d,t}$)	Log(Non-U.S. Resident Completions$_{d,t}$)
	(1)	(2)	(3)	(4)
Treated$_d$ × Post$_t$	-0.14***	-0.17***	-0.14***	-0.29***
	(-3.87)	(-4.83)	(-3.46)	(-4.19)
Degree FE	Yes	Yes	Yes	Yes
Year FE	Yes	Yes	Yes	Yes
Observations	10,980	10,980	9,044	9,044
R-squared	0.974	0.944	0.965	0.940

Appendix Table B5. **Tariff Exposure and Science & Engineering Employment in U.S. Chip Manufacturing Companies**

This table presents our findings on the influence of U.S. protectionism on science and engineering employment across industries with varying levels of tariff exposure. Tariff data is sourced from Fajgelbaum et al. (2020), and industry concordance is based on Pierce and Schott (2012). Additional definitions can be found in Section **??**. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by ⋆⋆⋆, ⋆⋆, and ⋆, respectively.

	Panel A: High Tariff Exposure		Panel B: Low Tariff Exposure	
	$\text{Log}(\text{Emp}_{i,j,t})$	Net Hiring $\text{Rate}_{i,j,t}$	$\text{Log}(\text{Emp}_{i,j,t})$	Net Hiring $\text{Rate}_{i,j,t}$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.04***	-0.02**	-0.02**	-0.01**
	(-2.79)	(-2.38)	(-2.03)	(-2.32)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	39,447	39,447	29,502	29,502
R-squared	0.973	0.356	0.978	0.308

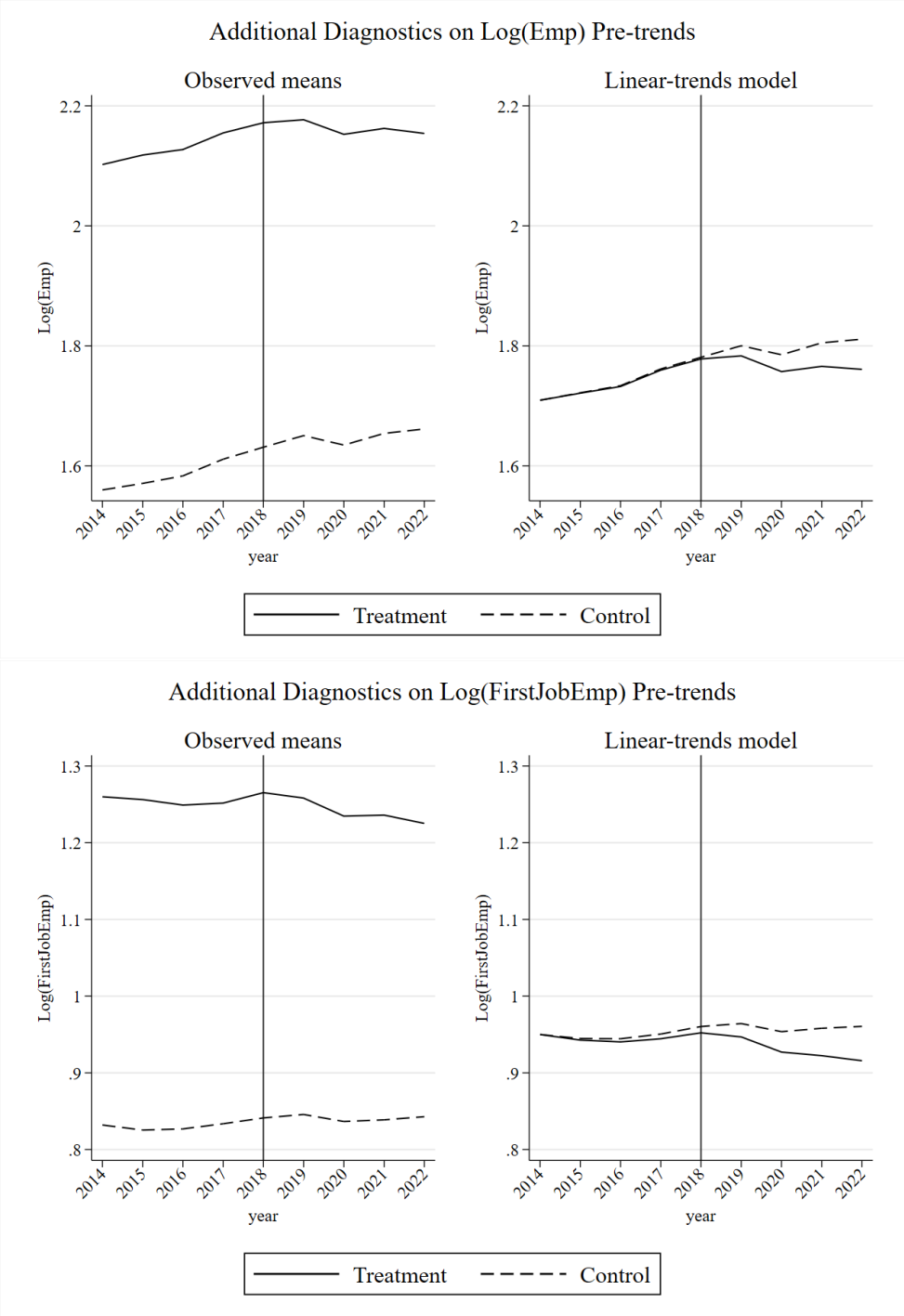
Appendix Table B6. **Main Findings From Poisson Regression Analysis**

This table presents our findings on how U.S. protectionism has influenced science and engineering employment at U.S. chip manufacturing companies. Our estimates are derived from a Poisson pseudo-likelihood regression with multiple levels of fixed effects. To ensure the mean and variance of the dependent variables are similar, we take the logarithm of the dependent variables and apply probability weights, calculated as the inverse of each firm's workforce size in 2014. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively. The analysis spans from 2014 to 2022, with standard errors clustered by firm. Significance levels of 1%, 5%, and 10% are denoted by $\star\star\star$, $\star\star$, and $\star$, respectively.

	$\text{Log}(\text{Emp}_{i,j,t})$	$\text{Log}(\text{Hiring}_{i,j,t})$	$\text{Log}(\text{Separation}_{i,j,t})$	$\text{Log}(\text{Turnover}_{i,j,t})$
	(1)	(2)	(3)	(4)
$\text{Treated}_j \times \text{Post}_t$	-0.07***	-0.11***	-0.09*	-0.11**
	(-3.24)	(-2.67)	(-1.67)	(-2.56)
Firm × Job Category FE	Yes	Yes	Yes	Yes
Firm × Year FE	Yes	Yes	Yes	Yes
Observations	68,598	68,598	68,598	68,598

Appendix Figure B1. **Additional Trend Diagnostics**

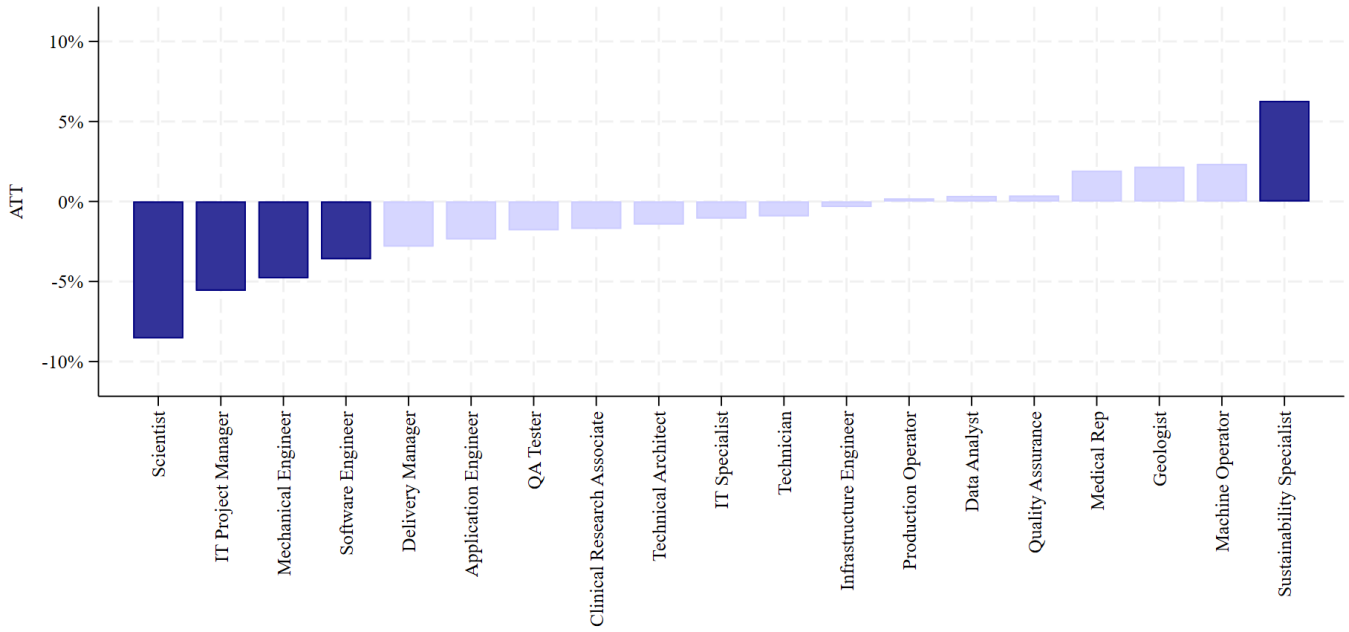
This figure provides additional diagnostics for the pre-trends in our main difference-in-differences estimation. The first panel displays data on *Log(Emp)*, while the second panel focuses on *Log(FirstJobEmp)*. Both panels present observed means along with linear trends derived from Stata's `xtdidregress` command. For the linear trends model, we incorporate firm × job category, and year fixed effects.



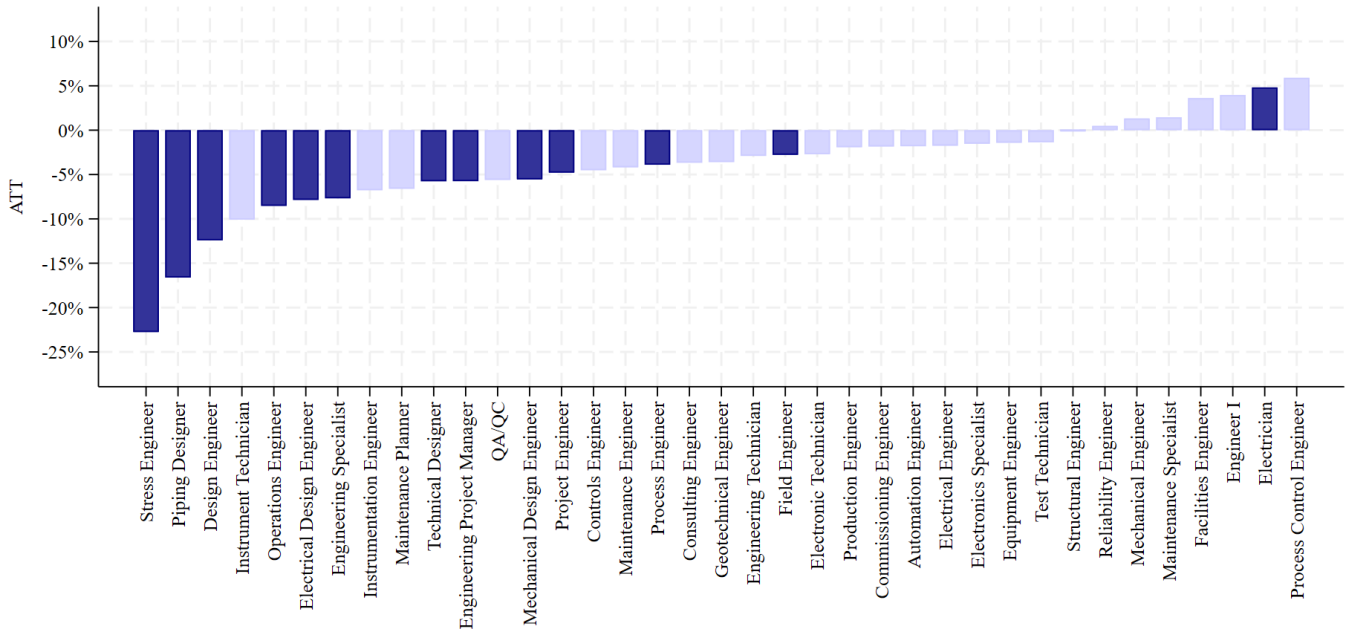
Appendix Figure B2. **Effect Heterogeneity Across Job Categories**

This figure presents additional evidence of effect heterogeneity across Revelio's job categories. Instead of using our primary definition of treated units—scientist and engineering roles within a firm—we refine the treatment definition by using Revelio's role_k50 classification in Panel A. In Panel B, we show the effect heterogeneity for roles labeled as *Mechanical Engineer* positions in Panel A by using Revelio's role_k1000 subcategories. In both panels, we compare the treated categories to control units, which are non-engineering and non-scientist jobs within the same firm and year, based on Specification (9) and Table 5. Therefore, the estimated ATTs are conditional in the sense that they measure the treatment effects only for firms that employ individuals in each role_k50 or role_k1000 category. The y-axis shows the average treatment effects from our analysis. Bars in darker blue represent statistically significant effects at the 10% level or higher, while light blue bars indicate effects that are not statistically significant.

Panel A: Heterogeneous Effects on Job Categories Using Revelio's Role_k50 Classification

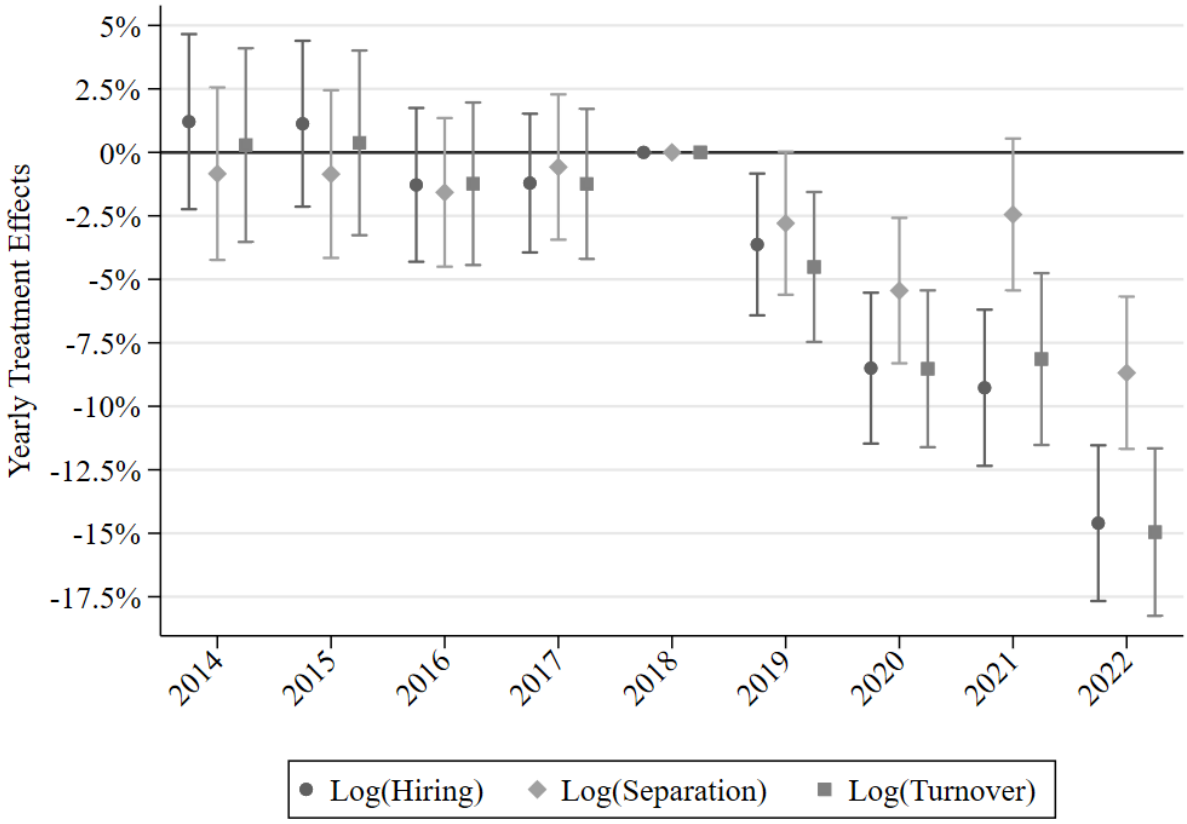


Panel B: Heterogeneous Effects on Mechanical Engineering Jobs Using Revelio's Role_k1000 Classification



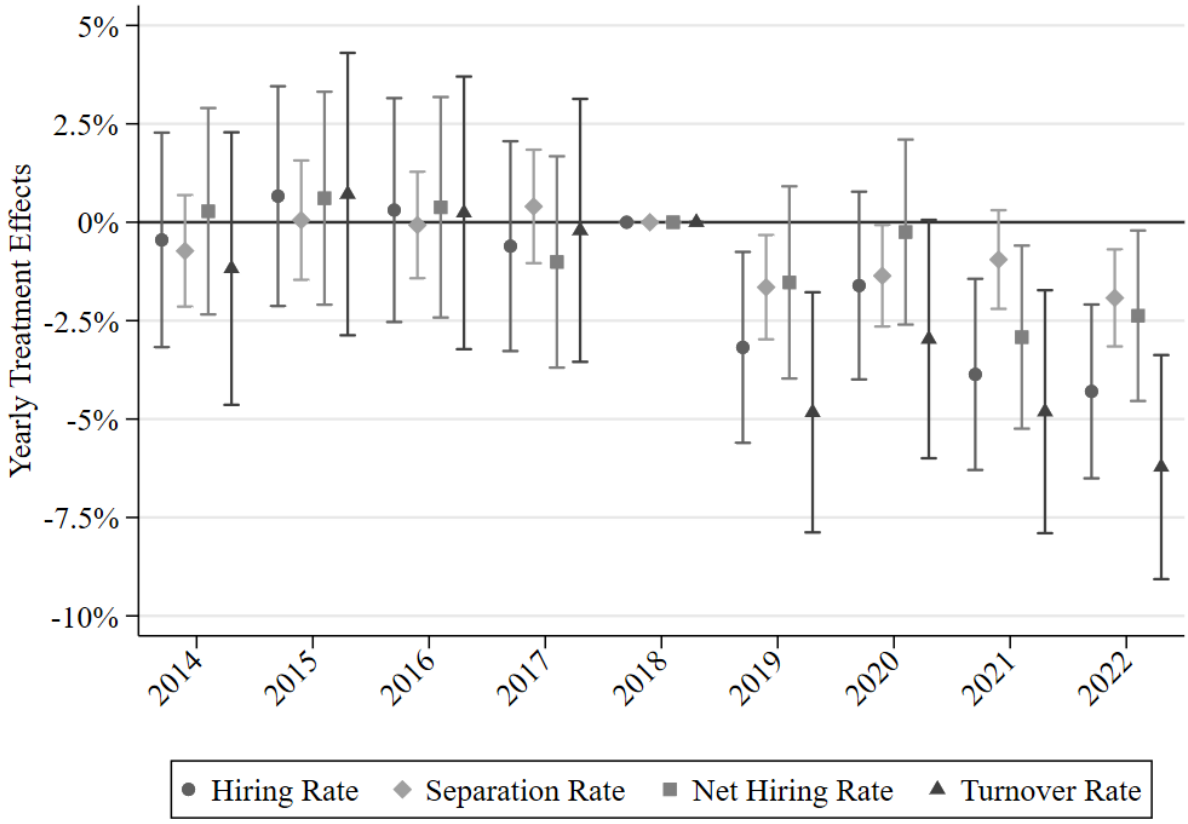
Appendix Figure B3. **Effect Dynamics: Table 5, Panel A**

The figure illustrates the dynamic effects on all other dependent variables listed in Panel A of Table 5 that have not been included in the main text. These effects are calculated using a difference in differences model as in specification (9), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively.



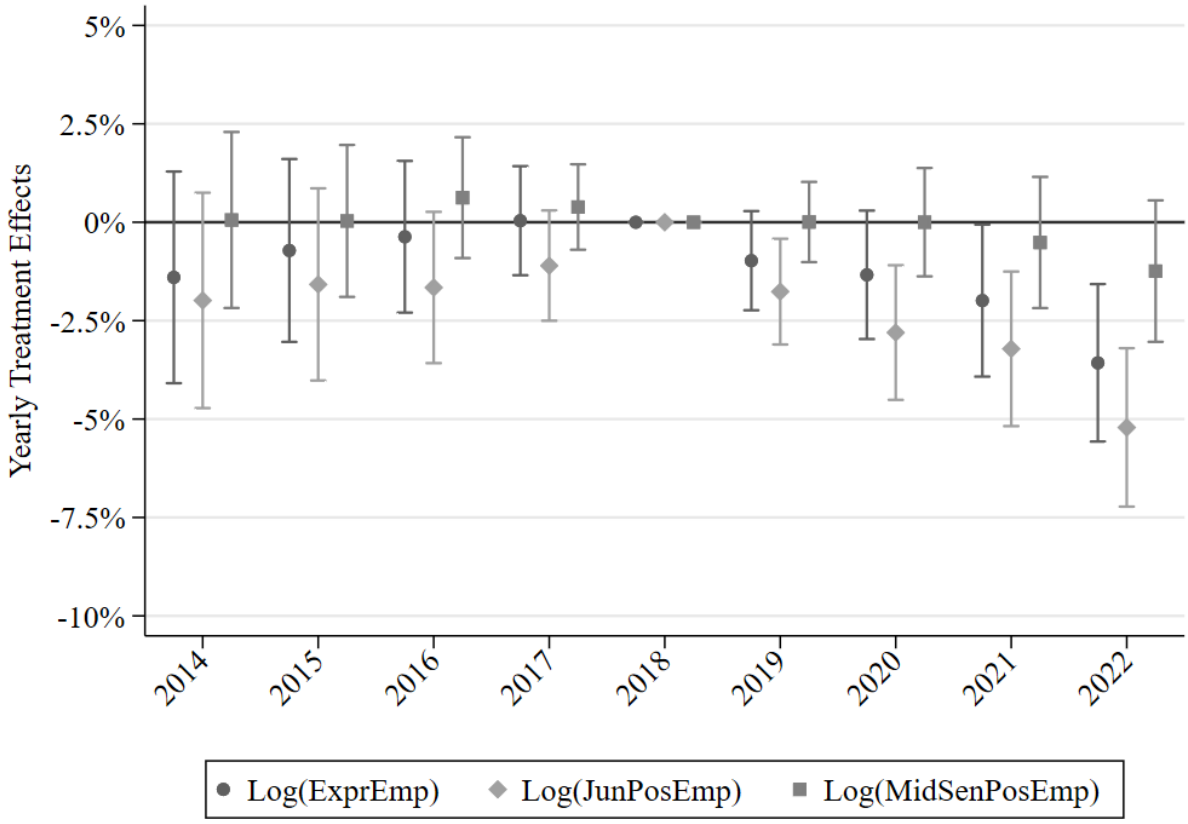
Appendix Figure B4. **Effect Dynamics: Table 5, Panel B**

The figure illustrates the dynamic effects on all other dependent variables listed in Panel B of Table 5 that have not been included in the main text. These effects are calculated using a difference in differences model as in specification (9), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively.



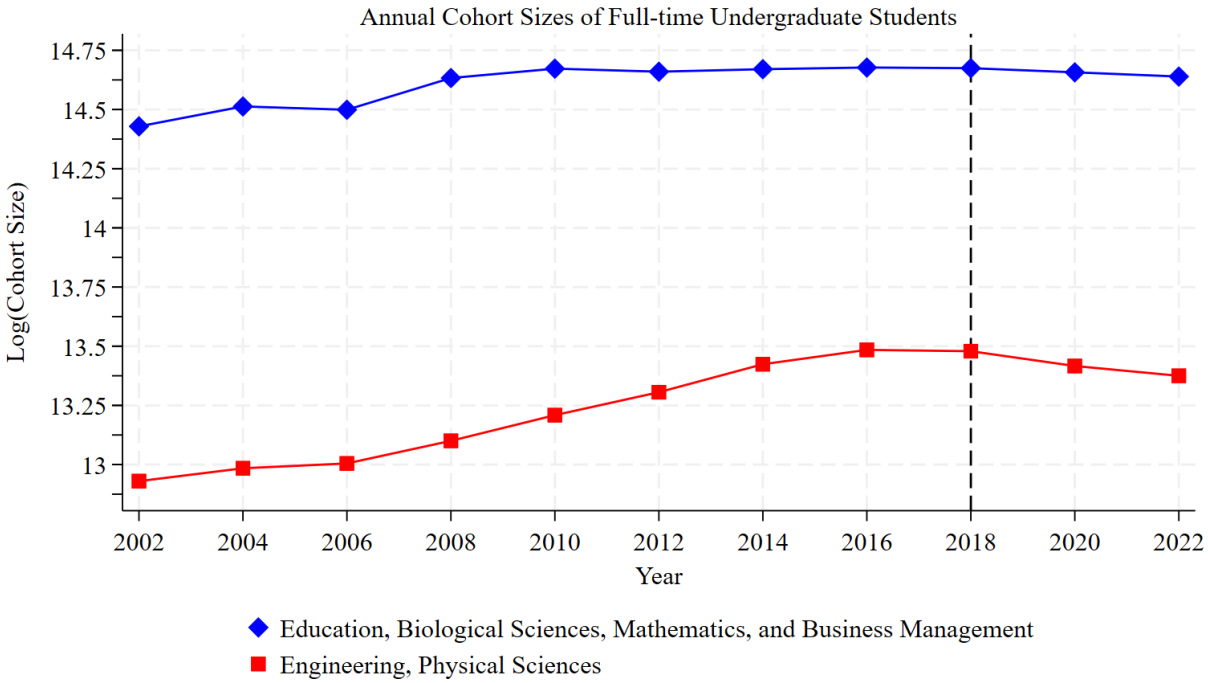
Appendix Figure B5. **Effect Dynamics: Table 6**

The figure illustrates the dynamic effects on all other dependent variables listed Table 6 that have not been included in the main text. These effects are calculated using a difference in differences model as in specification (9), which controls for both firm × job category and firm × job year dummies. Each point estimate is accompanied by a 95% confidence interval. For information on how data was collected and definitions of the variables used, refer to Sections B.1.3 and B.2, respectively.



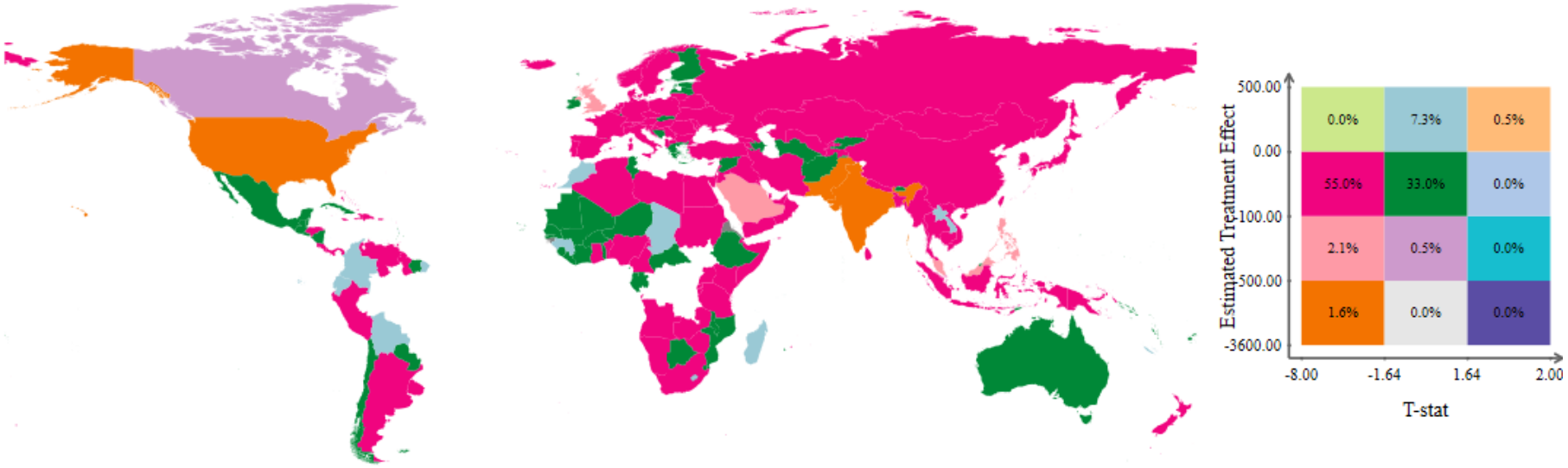
Appendix Figure B6. **Full-Time Undergraduates: U.S. Department of Education Data**

This figure illustrates the logged total number of full-time undergraduate students in the U.S., derived from biannual Fall Enrollment surveys conducted by the Integrated Postsecondary Education Data System (IPEDS) under the U.S. Department of Education. The category "Engineering and Physical Sciences" includes all programs with CIP codes 14.0000 and 40.0000, while "Education, Biological Sciences, Mathematics, and Business Management" encompasses programs with CIP codes 13.0000, 26.0000, 27.0000, and 52.0000. Full-time undergraduate students are defined by the value of 'lstudy' equal to 22.



Appendix Figure B7. **Effect Heterogeneity: Shift Away from Science and Engineering Roles**

This figure displays the results of applying Equation (12) separately for each country to analyze the effect of U.S. protectionism on classmates of individuals skilled in chip manufacturing securing science and engineering positions. We focus on the peers of those with chip manufacturing skills, considering only those who graduated in the same year, pursued the same degree, and resided in the same country. Our examination covers their career paths both before and after the beginning of U.S. protectionism in 2018. The analysis is visualized on a bivariate world map, where the subsample effects are shown on the y-axis and the p-values of these estimated effects on the x-axis, with different color labels distinguishing the results. The matrix within the figure indicates the percentage of countries falling into each category, written in black. Countries with no data are shown in white.



Appendix Figure B8. **Effect Heterogeneity: Global Workforce Trends in U.S. Chip Manufacturers**

This figure shows the outcomes of using Equation (10), incorporating fixed effects only for firm by country by job category and firm by year, with each country analyzed separately. The results are shown visualized on a bivariate world map, where the estimated effects are shown on the y-axis and the t-stats of these estimated effects on the x-axis, with different color labels distinguishing the results. The matrix within the figure indicates the percentage of countries falling into each category, written in black. Countries with no data are shown in white.